373 Final Review

Timer & PWM

Terminology and functionality of timer

- **Compare**: trigger event at certain time. hardware timer usually has dedicated compare register.

```
// function prototype in C.
// they are used when you want callback_fn to be called at a specific time
void alarm (callback_fn, delta);
void alarm (callback_fn, actual time);
```

- **Capture**: record timestamp. Like compare, hardware timer usually has dedicated capture register.

```
// get the current time
time_t curr_time;
curr_time = time(null);
```

- **Overflow**: timer value wraps around.
- **Prescaler**: a divider to slow down a higher clock frequency.

Common application:

- Virtual timer
- Watchdog timer (generates non-maskable interrupt)
- Accurate delay in embedded system program
- **Pulse width modulation**

ADC & DAC

Terminology of ADC & DAC

- **resolution**: total number of discrete values. Usually represented as # of bits. >10 bit ADC has resolution of 2^10 = 1024
- **step / LSB**: reference voltage divided by resolution. >V_ref = 3.3 V >resolution = 1024 >step = 3.3 / 1024 V

* **quantization error**: largest difference between represented value and actual value.

    least quantization error is 1/2 LSB. * **differential nonlinearity (DNL)**: The largest possible difference between actual step size and ideal step size. Assume 2 bit ADC with

V_ref of 4 volts Step is 1 volt In theory, this adc would convert 0.5 - 1.5 V into 0x01. For some manufacturing errors, a batch of this kind of ADC acutally convert 0.3 - 1.8 V into 0x01. The DNL for those ADC is 0.5 V (1/2LSB). * **integral nonlinearity (INL)**: It is the deviation of the transfer function from a straigt line. For DAC, it is the largest possible difference between ideal output value and actual output value for a specific input code. (eg. When you input 0x01, you expect the output to be 1 volt, the DAC instead outputs 1.2 volt. The INL is 0.2 V.) For ADC, it is the largest possible difference between ideal input threashold value and the actual input threashold value for an output code. (eg. If you want to get 0x01, the ideal minimum input voltage is 0.5 volt. However, you notice that when you input 0.1 volt, the output of the ADC is 0x01. The INL is 0.4 V.)

NOTE: INL is usually a more effective measurement than DNL, because INL is the worst difference between actual output and desired output. If you are only given DNL, there's no guarantee for the worst case difference, because INL is integral of DNL.

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opamp

Important features of an ideal opamp:

- Gain is ∞, so **the input voltages are the same**. (Otherwise there is a non-zero difference, the output would be infinity)
- The input impedance is also ∞, so **the currents are both 0**.

Practice

1. 100 clock ticks of a 100Mhz clock takes about __ ns.
2. 
3. 

Reference

http://www.eecs.umich.edu/courses/eecs373/lectures/l8.pdf
http://www.eecs.umich.edu/courses/eecs373/lectures/l10.pdf
http://www.eecs.umich.edu/courses/eecs373/lectures/l15.pdf