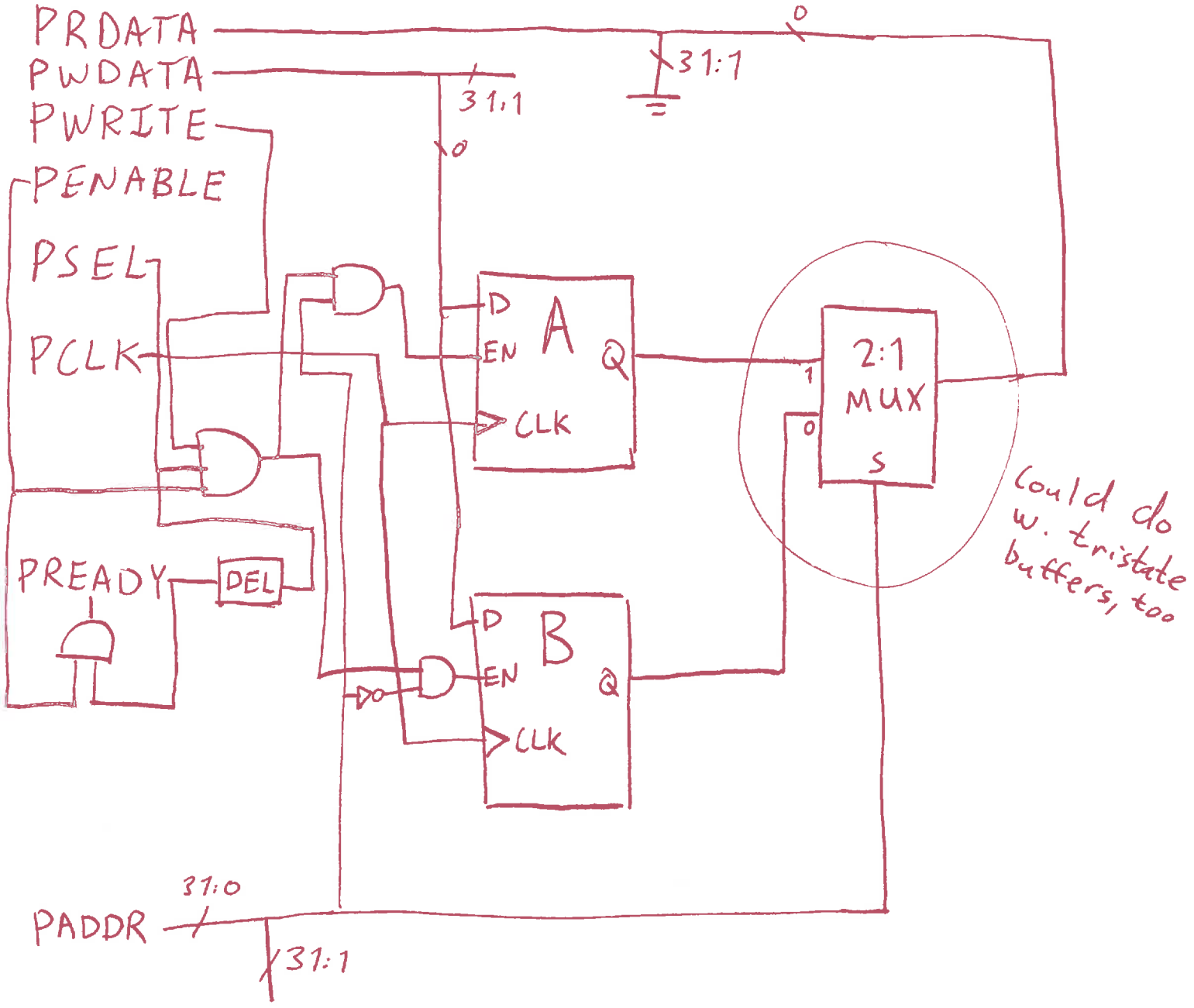
Notes on These Examples

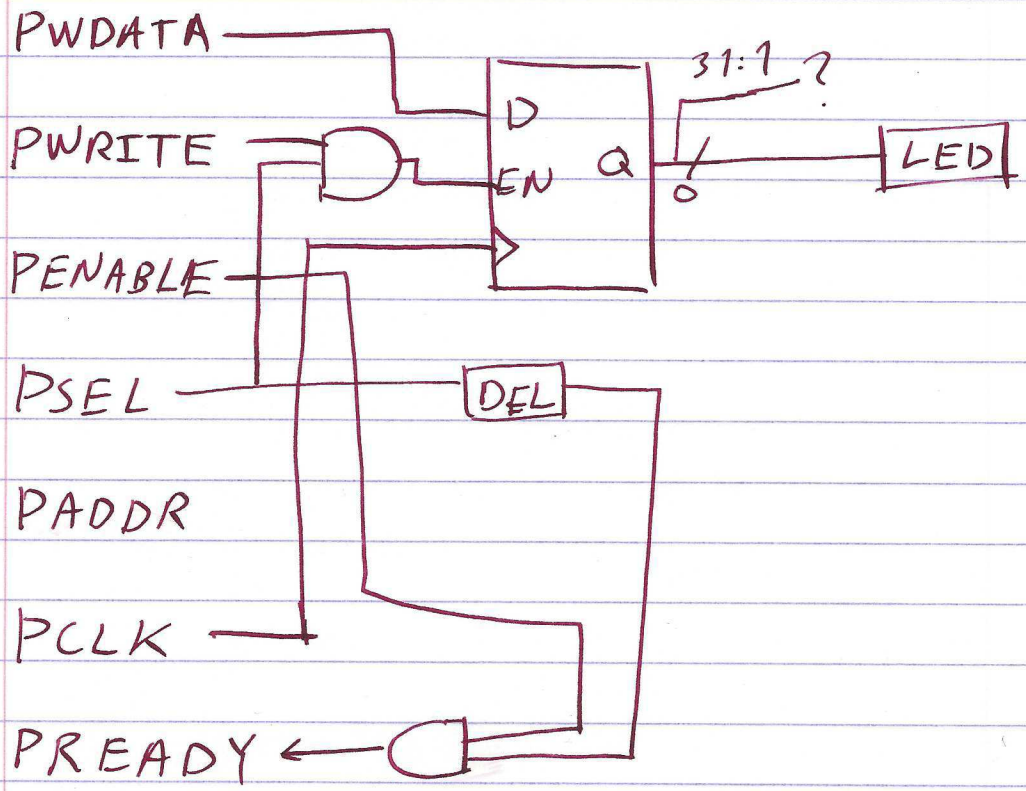
The APB3 specification describes separate PRDATA and PWDATA buses. They cannot be used at the same time, however, because control signals are shared among them. It would be possible to implement a version with those interconnects shared, but wouldn't make much sense except in an off-chip application, and is not recommended by ARM. Assume they are not shared.

Now it gets stranger. The same PWDATA wires are connected to each peripheral. However, every peripheral has its own set of PRDATA lines. That means there are a lot of wires going into the master. This would be a bit crazy for off-chip applications but for on-chip applications the routing cost is offset by a significant benefit: there is no need to tristate the outputs of peripherals.

Here are the implications. These examples will work for a bus with shared or unshared data lines and it is important to understand the concept of using device tristate buffers to prevent short circuits. But they could be simplified further if used for our development board. How? Cross out any tristate buffers and their control logic, and just use wires. Finally, this is rare for low-performance buses, especially off-chip buses, so do make sure you understand why tristate buffers often need to be used. You will encounter such buses in the future.

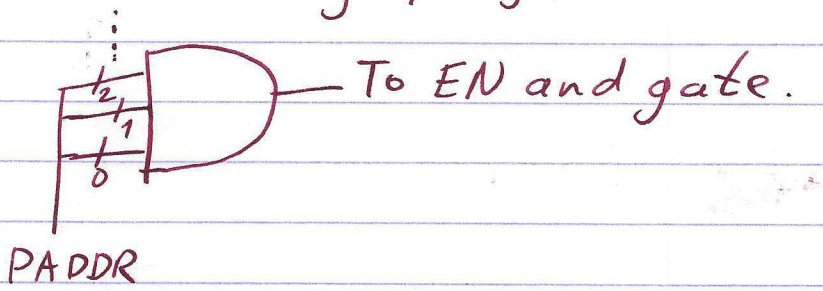
Write/Read A when PADDR is odd, B when PADDR is even. This only uses bit 0.



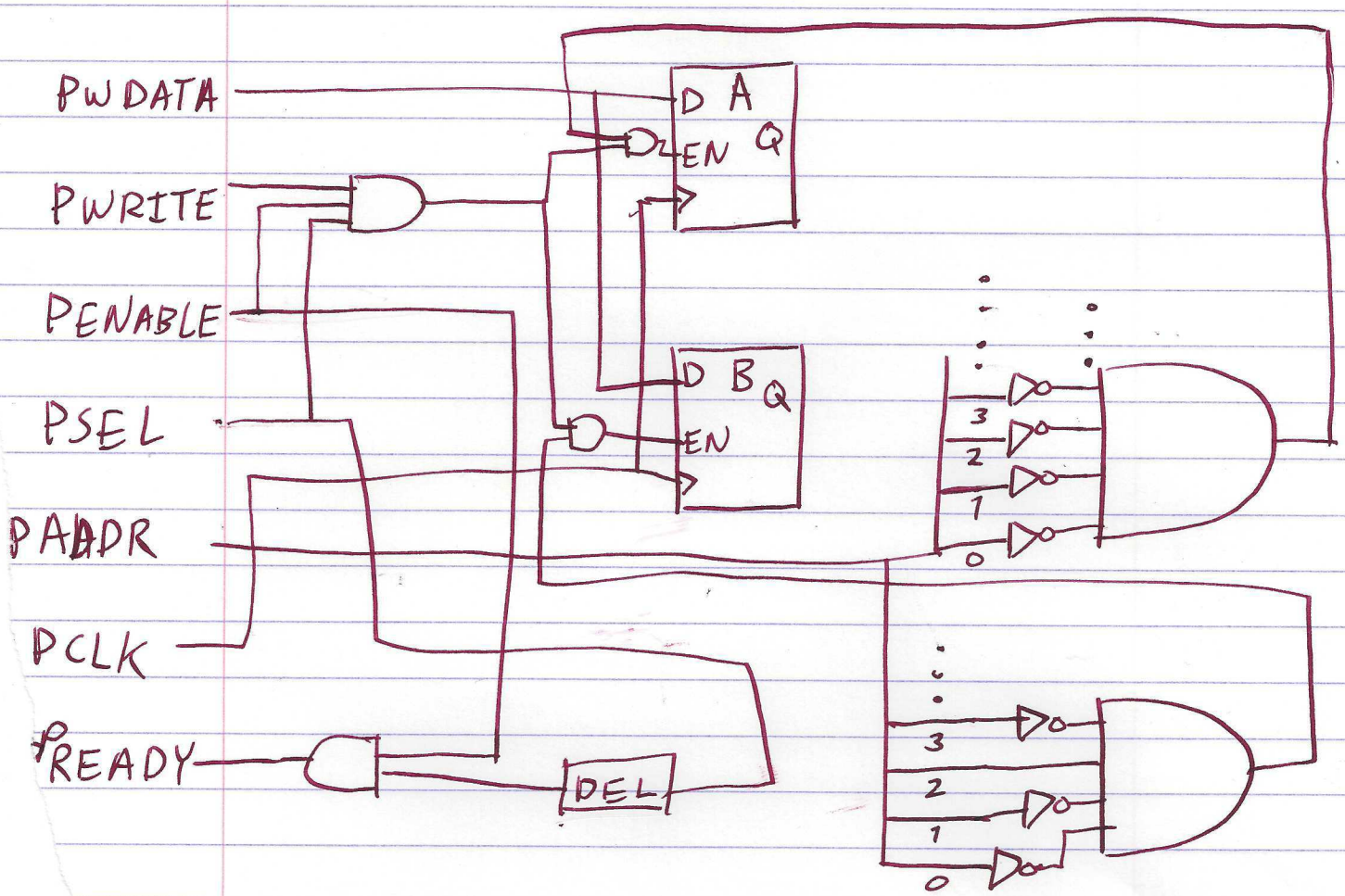


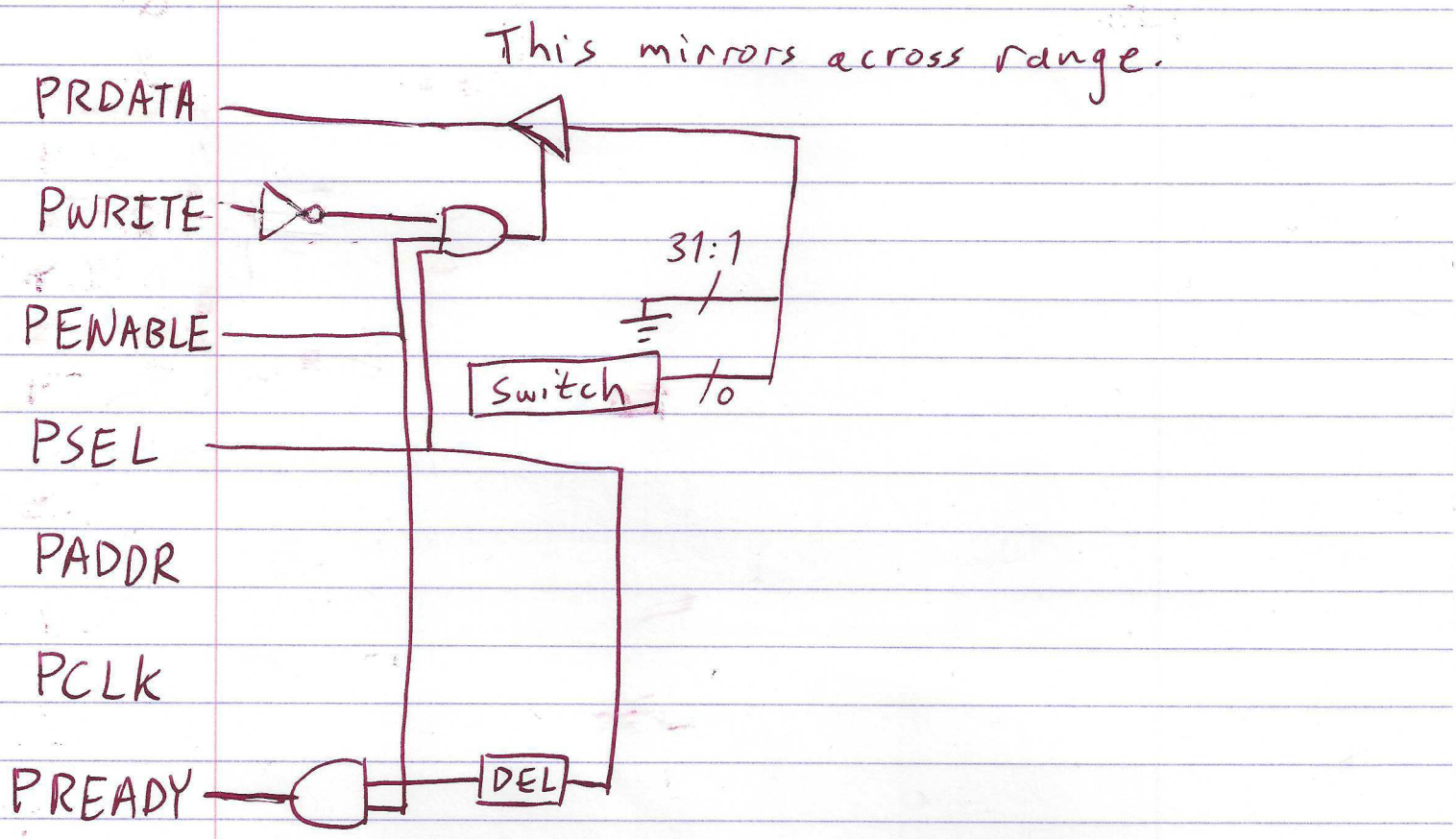
Assuming PSEL high for address range assoc w. device.

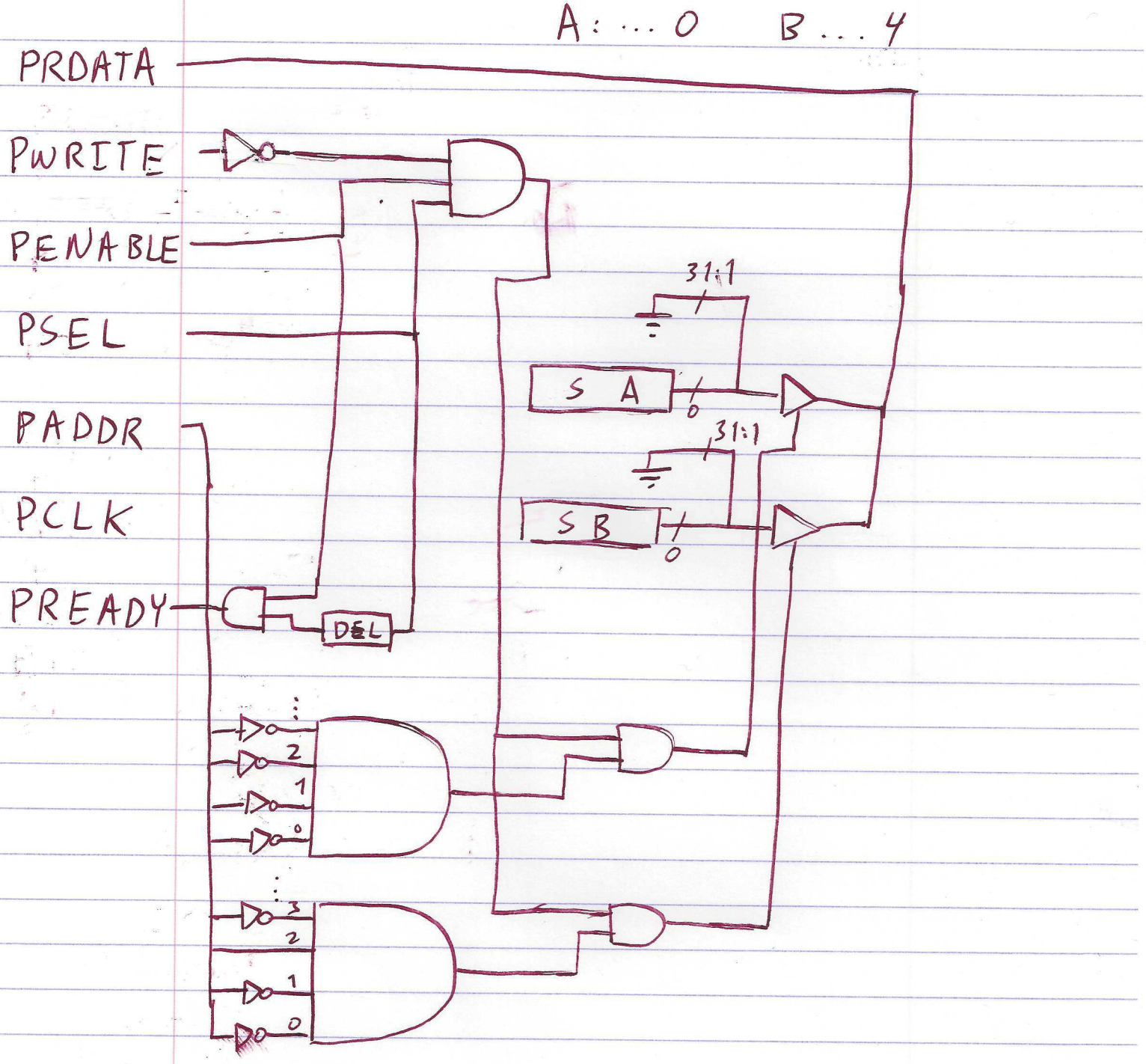
PADDR could be used to prevent mirroring within range, e.g.:

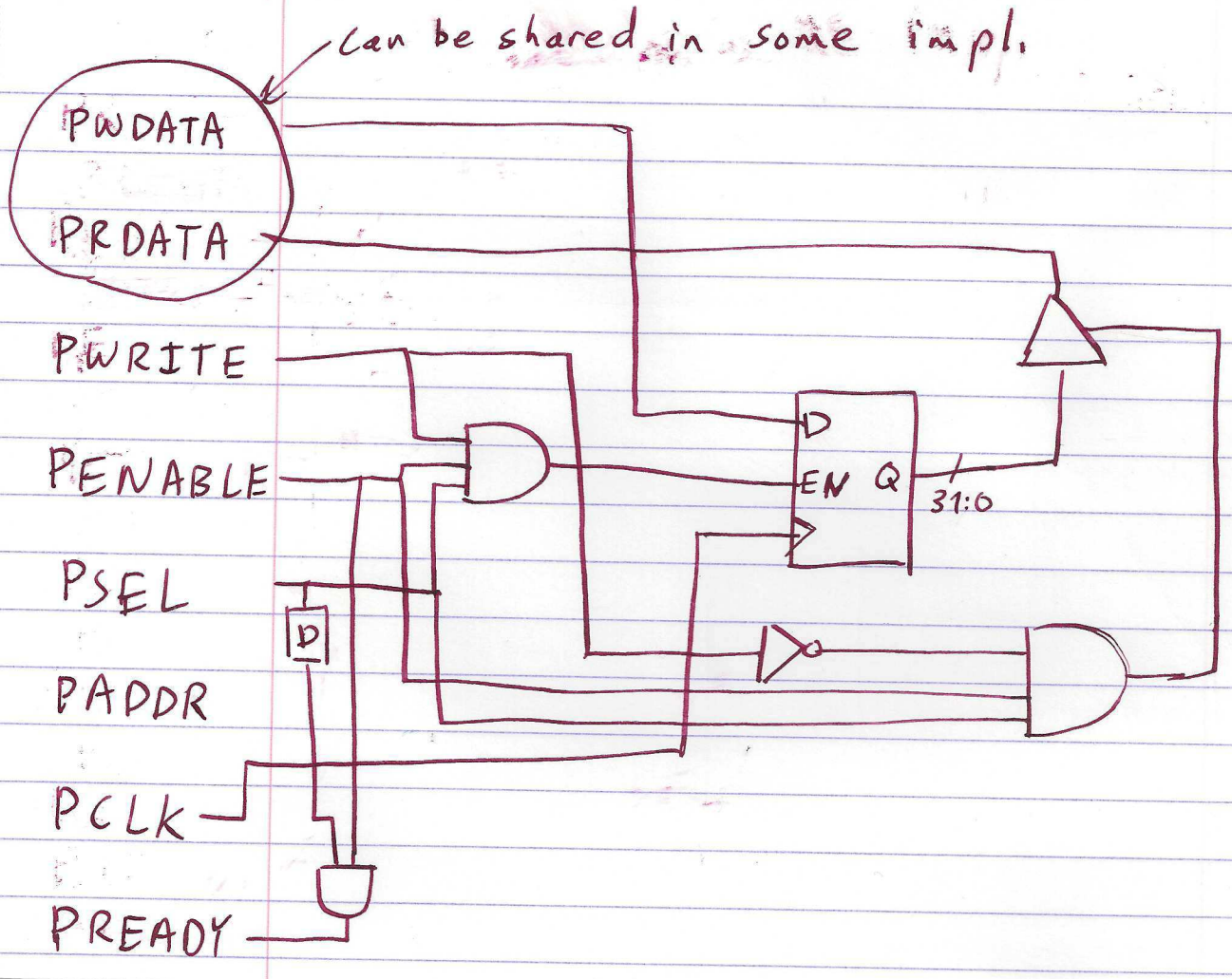


A : 0x00001000
B : 0x00001004




This mirrors across range.
PRDATA
PWRITE
PENABLE
PSEL
PADDR
PCLk
PREADY
31:1
switch
to
DEL


A: ... 0
B ... 4
PRDATA
PWRITE
PENABLE
PSEL
PADDR
PCLK
PREADY
DEL
31:1
S A
0
31:1
S B
0
2
1
0
3
2
1
0


can be shared in some impl.
PWDATA
PRDATA
PWRITE
PENABLE
PSEL
PADDR
PCLK
PREADY
D
EN
Q
31:0