University of Michigan **EECS 373**
Fall 2001

EXAM 2

Instructions

1. This is an open books/notes exam.
2. It comprises 25 multiple-choice questions, each worth 4 points.
3. Each question has only one correct answer.
4. For each question, indicate your answer on the answer sheet provided.
5. You have 75 minutes to complete the exam.
6. Please make sure you enter your name in the space below AND on the answer sheet.
7. By signing below, you certify that your conduct throughout the exam has been in accordance with the College of Engineering Honor Code.
8. At the end of the exam, please turn in this exam booklet AND your answer sheet.

Name _____

Signature _____

Memories and Buses [16 points]

Questions 1—2 refer to a 64Kbit memory with a square physical configuration and an external configuration of 16K x 4.

1. What size is the demux at the memory output?

    a. 8:4
    b. 64:4
    c. 128:4
    d. 256:4
    e. None of the above

2. How many address bits are supplied to the memory?

    a. 8
    b. 14
    c. 16
    d. 20
    e. None of the above

Questions 3—4 refer to a semisynchronous bus in which each read transaction consists of an address transfer followed by a word transfer. Each address transfer takes 4 cycles and each word transfer takes 2 cycles. The bus clock is 50MHz. As usual, 1 word = 4 bytes.

3. What is the bandwidth of the bus for single-word transfers? (Assume $10^9 \sim 2^{30}$)

    a. 1/2 Gbytes/sec
    b. 1/10 Gbytes/sec
    c. 1/20 Gbytes/sec
    d. 1/30 Gbytes/sec
    e None of the above

4. What is the bandwidth if single-word accesses are pipelined so that the address transfer of each transaction overlaps with the data transfer of the preceding one?

    a. 1/2 Gbytes/sec
    b. 1/10 Gbytes/sec
    c. 1/20 Gbytes/sec
    d. 1/40 Gbytes/sec
    e. None of the above

Procedures and ABIs [20 points]

5. A program that complies to the MPC823 ABI has the following three functions:

   - Main: Where program execution begins and ends. Nothing calls Main.
   - Foo: A function that is called only by Main and calls only one function Bar.
   - Bar: A leaf function that is called only by Foo. Bar calls no other function.

   If `r14` is used in Main to hold an important variable and both Foo and Bar use `r14` for calculations, which functions will save `r14` so that both Main and Foo are guaranteed to find the value they expect in `r14` after they perform a function call?

   a. Main and Foo both save `r14`
   b. Foo and Bar both save `r14`
   c. Only Foo saves `r14`
   d. Only Bar saves `r14`
   e. Only Main saves `r14`

6. Suppose you are writing a program compliant to the MPC823 ABI and that you need to call an ABI-compliant function that another group in 373 is responsible for writing. You have no clue how their function works, but you must make a few assumptions on how it should be called. Their function expects three parameters: Years, Months, and Days in that order. It will be returning the value Seconds. In which locations do you place the parameters, and where can you expect to find the return value?

   a. Parameters: `r0`, `r1`, `r2` Return Value: `r3`
   b. Parameters: `r3`, `r4`, `r5` Return Value: `r6`
   c. Parameters: `r4`, `r5`, `r6` Return Value: `r3`
   d. Parameters: `r3`, `r4`, `r5` Return Value: `r3`
   e. Parameters: In stack frame Return Value: `r3`

7. Functions can avoid saving many registers on the stack by carefully selecting the registers they use to store values. Assume there are three types of MPC823 ABI-compliant functions called top, middle, and leaf such that top is only a caller, leaf is only a callee, and middle is both a caller and a callee. Which of the following register usage schemes minimizes the amount of registers saved to the stack? Assume there are enough volatile or non-volatile registers to save all values in use.

   a. Top: Non-Volatile Registers
   Middle: Non-Volatile Registers
   Leaf: Volatile Registers

   b. Top: Volatile Registers
   Middle: Volatile Registers
   Leaf: Non-Volatile Registers

   c. Top: Volatile Registers
   Middle: Non-Volatile Registers
   Leaf: Volatile Registers

   d. Top: Non-Volatile Registers
   Middle: Non-Volatile Registers
   Leaf: Non-Volatile Registers

   e. Top: Volatile Registers
   Middle: Volatile Registers
   Leaf: Volatile Registers

8. Which of the following statements are always true about the MPC823 ABI?

   I. The Condition Registers must be saved by the Caller
   II. The Link Register should be saved by the Caller
   III. The stack pointer is in `r1`
   IV. A callee must save **all** Non-Volatile registers

   a. I, III, IV
   b. II, III, IV
   c. II, III
   d. III
   e. None

9. Indicate which of the choices below correctly complete the following statement: "An ABI-compliant object file…"

    I. can call system library routines
    II. can be called by other ABI-compliant code
    III. can be used with different operating systems
    IV. can be used with different ABI-compliant compilers

    a. I and II
    b. I , II, and III
    c. II and IV
    d. III and IV
    e. I, II, and IV

Interrupts and Timers [32 points]

10. Which of the following events automatically (i.e., without any action by the ISR) take place every time an external interrupt occurs on the MPC823?

    I. The return address of the interrupt is saved in SRR0, and the MSR is saved in SRR1.
    II. The link register is updated.
    III. External interrupts are disabled.
    IV. The appropriate bit in SIPEND is set to 0.

    a. I and IV
    b. I, II, and IV
    c. I and III
    d. I, III, and IV
    e. I, II, III, and IV

11. Assuming you wish to be able to debug your ISR, which of the MPC823 registers listed below will always need to be saved as part of your ISR prologue code?

    I. The link register
    II. The condition register
    III. SRR0 and SRR1
    IV. All callee-save registers used in your ISR and/or handlers
    V. All general-purpose registers used in your ISR and/or handlers

    a. I, III, and V
    b. I, II, and IV
    c. II and V
    d. II, III, and V
    e. II, III, and IV

12. Which of the following MPC823 device registers must be configured to generate a real-time clock interrupt? (The list may be incomplete. Assume the key registers have been enabled.)

    I. IMMR
    II. SIMASK
    III. SCCR
    IV. SIPEND
    V. RTCSC

    a. I, III, and V
    b. II, III, and V
    c. I, II, IV, and V
    d. I, II, III, and V
    e. II, III, IV, and V

13. Assume that you are handling a Timer 1 reference interrupt (i.e., TCN1 == TRR1) on the MPC823 as in Lab 7. Each item in the following list describes an event necessary to handle the interrupt correctly. What is the order in which these events must occur?

    I. Set the IACK bit in the CIVR, then read the CIVR for the CPIC interrupt vector.
    II. Clear the appropriate bit in the CISR.
    III. Clear the REF bit in TER1.
    IV. Read SIVEC to determine the SIU interrupt source.
    V. Branch to the Timer 1 interrupt handler (i.e., the code that updates the chaser display).

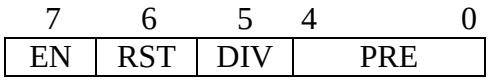
    a. IV, I, V, III, II
    b. IV, I, V, II, III
    c. IV, V, I, III, II
    d. IV, V, I, II, III
    e. None of the above

14. Which of the following statements about the MPC823 are true?

I. You can set breakpoints in an ISR or handler at any point after you save SRR0 and SRR1.
II. In order to clear RTC interrupts, all you have to do is clear the appropriate bit in SIPEND.
III. If the MSR is not configured correctly, then your top-level ISR will not be looked up at 0x0500.
IV. To access the SIU registers (SIVEC, SIPEND, SIMASK), you can use the `mtspr` and `mfspr` instructions.

a. I
b. I and II
c. III
d. I, III, and IV
e. None of the above

For Questions 15—17, assume you are given a system which contains an 8-bit timer that consists of three 8-bit registers: a count register (CNT) which holds the count value of the timer, a reference register (REF), and a control register (CTL). The control register CTL is configured as follows:



- EN: Must be set to 1 for the timer to be enabled.
- RST: If this bit is set to 1, the count register will reset to 0 every time the count value reaches the reference value. Otherwise, the timer will continue to increment when the reference value is reached.
- DIV: Setting this bit to 1 divides the system clock by 16 to produce the input clock frequency. If DIV = 0, then the input clock frequency equals the system clock frequency.
- PRE: A 5-bit prescaler; the timer frequency is equal to:

$$\frac{Input\ clock\ frequency}{(PRE+1)}$$

The timer generates an interrupt every time the count register reaches the value in the reference register REF. The system clock frequency is 10 MHz.

15. What is the slowest rate at which the timer can be incremented?

    a. 625 kHz
    b. 322.58 kHz
    c. 312.5 kHz
    d. 20.16 kHz
    e. 19.53 kHz

16. Assuming that the timer is running at its maximum frequency (i.e. incrementing as fast as possible), how long will it take to overflow?

    a. 0.1 microseconds
    b. 1.6 microseconds
    c. 25.5 microseconds
    d. 25.6 microseconds
    e. 409.6 microseconds

17. Which of the following settings will set the timer to generate an interrupt every 1.6 milliseconds?

    I. EN = 1, RST = 1, DIV = 1, PRE = 39, REF = 25
    II. EN = 1, RST = 1, DIV = 1, PRE = 19, REF = 50
    III. EN = 1, RST = 0, DIV = 1, PRE = 9, REF = 100
    IV. EN = 1, RST = 1, DIV = 1, PRE = 3, REF = 250
    V. EN = 1, RST = 1, DIV = 1, PRE = 5, REF = 200

    a. I, II, and IV
    b. I, II, III, and IV
    c. ***II and IV***
    d. I, II, IV, and V
    e. All of the above

ADCs and DACs [32 points]

Questions 18—25, pertain to a hypothetical analog-to-digital converter, the ADC0303. The ADC0303 is a 3-bit successive approximation A-to-D converter. Like the ADC0808, the ADC0303 has 8 analog channel inputs selected by the analog channel select register. The register is written/latched on the rising edge of the ALE control signal. When the conversion is complete, the ADC0303 can be read via its tri-state latch with the output enable signal OE. Table 1 gives specification data for the ADC0303. The DAC component of ADC0303 consists of the resistor ladder shown in Figure 1.

Minimum ALE Setup Time	Typical 25ns, Maximum 50ns
Minimum ALE Hold Time	Typical 15ns, Maximum 25ns
OE to Logic State	Typical 150ns, Maximum 200ns
Zero Error	-1/4 LSB
Full Scale Error	+1/4 LSB
Non Linearity	+/- 1/4 LSB
Clock Frequency	Min 10 kHz, Typical 640 kHz, Max 1380kHz

Table 1: Specifications for ADC0303.

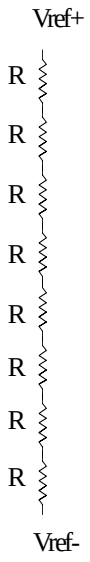


Figure 1: Resistor Ladder for DAC component of ADC0303

18. With Vref+ = 4.00 Volts and Vref- = 0.00 Volts, what **ideal** voltage range does the ADC0303 convert to 011b?

    a. 1.00 to 1.50 Volts
    b. 1.25 to 1.75 Volts
    c. 1.50 to 2.00 Volts
    d. 1.75 to 2.25 Volts
    e. None of the above

19. What is the minimum possible worst-case quantization error of this converter?

    a. 0.125 Volts
    b. 0.250 Volts
    c. 0.50 Volts
    d. 1 Volt
    e. None of the above

20. The voltage range that produces zero output for the ADC0303 is measured in the laboratory with a voltage divider and potentiometer. What is the smallest possible range of input voltage you might see?

    a. 0 to 0.125 Volts
    b. 0 to 0.250 Volts
    c. 0 to 0.375 Volts
    d. 0 to 0.500 Volts
    e. None of the above

21. The transition voltages of four ADC0303's are measured in the lab for the conversion values 101b and 110b. The results are as follows:

ADC	101b	110b
1	2.55 Volts	2.96 Volts
2	2.35 Volts	2.92 Volts
3	2.43 Volts	3.16 Volts
4	2.41 Volts	3.06 Volts

Which data sets were probably measured **incorrectly**?

    a. 1, 2, and 3
    b. 1 and 3
    c. 2 and 3
    d. 3 and 4
    e. None of the above

22. You are required to interface the ADC0303 to the MPC823 external bus. The bus clock is set to 20MHz. You must use the integral tri-state latch of ADC0303. What is the minimum number of wait cycles required to read the ADC0303?

a. 2
b. 3
c. 4
d. 5
e. None of the above

23. Your application requires selecting analog channel 0 and analog channel 1 on alternate samples. Assume that your hardware will generate ALE on the falling edge of TA*. What is the minimum number of wait states required to guarantee that the analog channel select register is properly written?

a. 0
b. 1
c. 2
d. 3
e. None of the above

24. Given a clock source of 20MHz, what binary output would you use from a 4 bit binary counter with output QaQbQcQd (LSB is Qa, MSB is Qd) to generate the fastest possible conversion clock?

a. Qa
b. Qb
c. Qc
d. Qd
e. None of the above

25. If the DAC component of the converter were implemented as an R/2R ladder, how many resistors would it contain?

a. 4
b. 6
c. 8
d. 10
e. 20