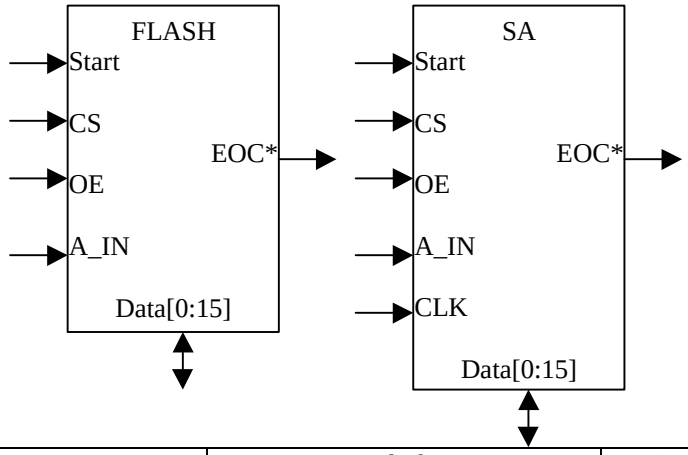
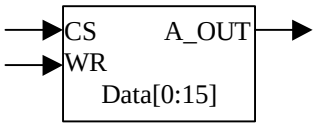
Answering Machine Component List (Problems 14 & 16)

ADC Converters

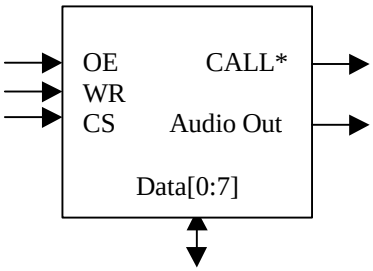


Converter Type	Flash	Successive Approximation
Converter CLK	NA	1kHz – 200kHz
Start Pulse width	300ns – 500ns	3us – 5us
Conversion time	2us	4 clock cycles
Cost	$0.75	$0.15

DAC Converter



Telephone Interface



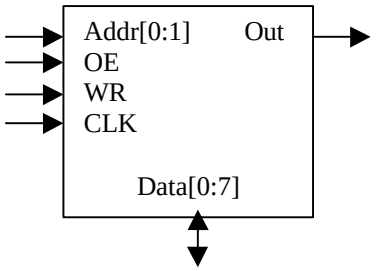
Register Map

0 - 4	5	6	7
reserved	Call	Hangup	Answer

Answer: (write only) 1 to answer phone, 0 to hang up
Hangup: (read only) 0 if connection is active, 1 if other party has hung up
Call*: (read/write) normally high (1), goes to 0 if there is an incoming call; CPU must write to clear. The state of this bit is reflected on the CALL* output signal as well.
Audio Out is an analog output carrying the audio signal from the telephone connection.

Answering Machine Component List (Problems 14 & 16)

Timer



Addr: Register	0	1	2	3	4	5	6	7
00: Control	Con0	Con1	RESV	RESV	Current	Switch	Enable	Out
01: Count	Count Value							
10: Reference 0	Reference Value 0							
11: Reference 1	Reference Value 1							

Control

Con0	Con1	Output Behavior
0	0	Toggle Out on match
0	1	Set High on match
1	0	Set Low on match
1	1	Do nothing

Current: Reference value being compared against
Switch: 0 – do nothing, 1—toggle Current on match
Enable: 1 – starts timer counting
Out: tied to output pin

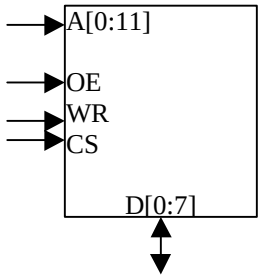
Count
Resets to zero when it reaches the reference value indicated by current

Reference 0/1
Reference values for comparing to Count.

Note: If you set both the Current and Switch bits to 0, the timer will only use Reference Value 0. In this case, you can treat it like a “normal” timer that has only one reference value.

Component List for Problem 13

4Kx8 SRAM

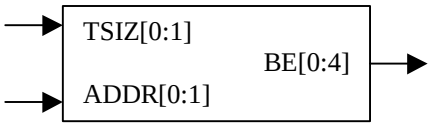


Access Times

All times are minimum times

OE to Read Data valid	15ns
CS to Read Data Valid	45ns
A stable to Read Data Valid	40ns
A stable to end of WR	40ns
WR pulse width	30ns
Data stable to end of WR	35ns
CS to end of write	30ns
Write cycle time	60ns

TSIZ Block



Delay: 8 ns

TSIZ [0:1]		Addr [0:1]		BE[0:3]			
0	0	0	0	1	1	1	1
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	1	0	0	0
0	1	0	1	0	1	0	0
0	1	1	0	0	0	1	0
0	1	1	1	0	0	0	1

TSIZ [0:1]		Addr [0:1]		BE[0:3]			
1	0	0	0	1	1	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	1	1
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

Any Logic Function Up To 3 Inputs

Delay: 4 ns

Answering Machine Block Diagram for Problems 14-16