READ AND FOLLOW THESE INSTRUCTIONS:

- Do not begin until you are told to do so.
- Write your name legibly on *every page*.
- You have two hours; budget your time. The questions are not of equal weight. Do not spend too much time on any one question, particularly if
- If you run out of space, continue working on the back of the *same* sheet.

This exam is *closed book, closed notes*. You may *not* refer to any reference materials; you should not need to. If you think you need to look something up, assume (i.e., make up) a reasonable answer and write down your assumption.

Honor Code statement: "I have neither given nor received aid on this exam."

Signature: _____

Question	Points	Score
1	3	
2	5	
3	9	
4	9	
5	12	
6	12	
7	50	
8	50	
9	50	
Total	200	

Questions 1-6 are short answer. Only the first two sentences of each part will be graded.

1. (3 pts) On PowerPC processors, as on all RISC architectures, loading an arbitrary 32-bit constant into a register requires two instructions. Why doesn't PowerPC have a single instruction that loads a 32-bit immediate value?

2. (5 pts) ABI

   a) What is the purpose of an application binary interface (ABI)?

   b) An ABI must specify several things to fulfill its purpose; for example, which register is used as the stack pointer. Name three other things specified by an ABI.

3. (9 pts) Memory types: You're designing a new digital set-top box for a next-generation high-definition cable TV system. For each of the data types listed, recommend a type of memory and list the key features of that memory type that make it the best choice for that application.

   a) Instructions (text segment): needs to be easily upgradable, at least 1 Mbyte

   b) Non-volatile storage for channel, volume, etc. settings, so that the device powers up in the same state as when it was powered off (less than 256 bytes)

   c) Video buffer for real-time special effects: at least 32 Mbytes, can be volatile

4. (9 pts) A/D, D/A conversion:

   a) What is monotonicity?

   b) What is differential non-linearity?

   c) If a converter is non-monotonic, what does this imply about its differential non-linearity?

5. (12 pts) Define the given terms.

   a) Embedded system

   b) Device driver

   c) Polling

   d) Aligned access (give a precise definition)

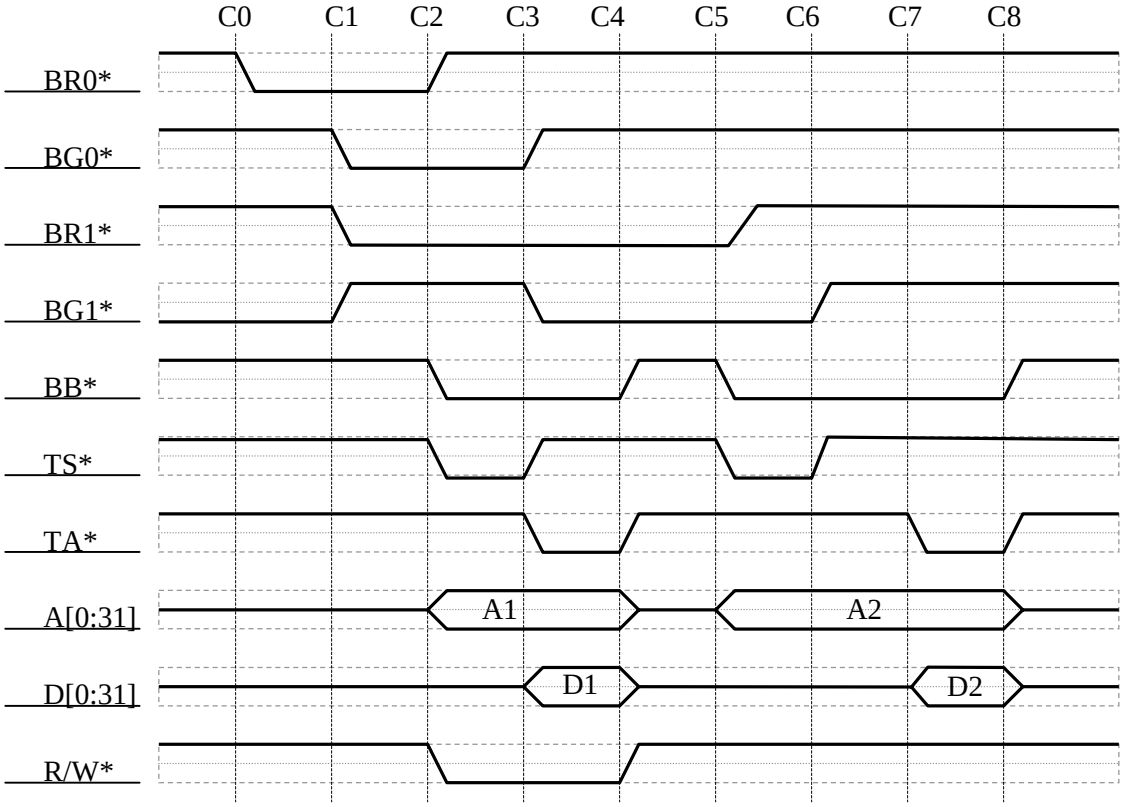
6. (12 pts) Busses & Interrupts
   a) What is a split-transaction bus?

   b) Is the MPC823 bus asynchronous, semi-synchronous, or synchronous?

   c) When an interrupt occurs in a system with true vectored interrupts, how is the interrupting device identified? List the primary advantage and primary disadvantage of this technique.

   d) If multiple devices generate interrupts simultaneously on a system with non-vectored interrupts, what determines which device will get serviced first?

7. Bus operation.
   a) The diagram below shows several cycles of activity on the MPC823 bus. The vertical dashed lines indicate the successive rising clock edges on which the bus signals are sampled. For each cycle, briefly describe what (if anything) is happening on that cycle.



Cycle	Description
C0	
C1	
C2	
C3	
C4	
C5	
C6	
C7	
C8	

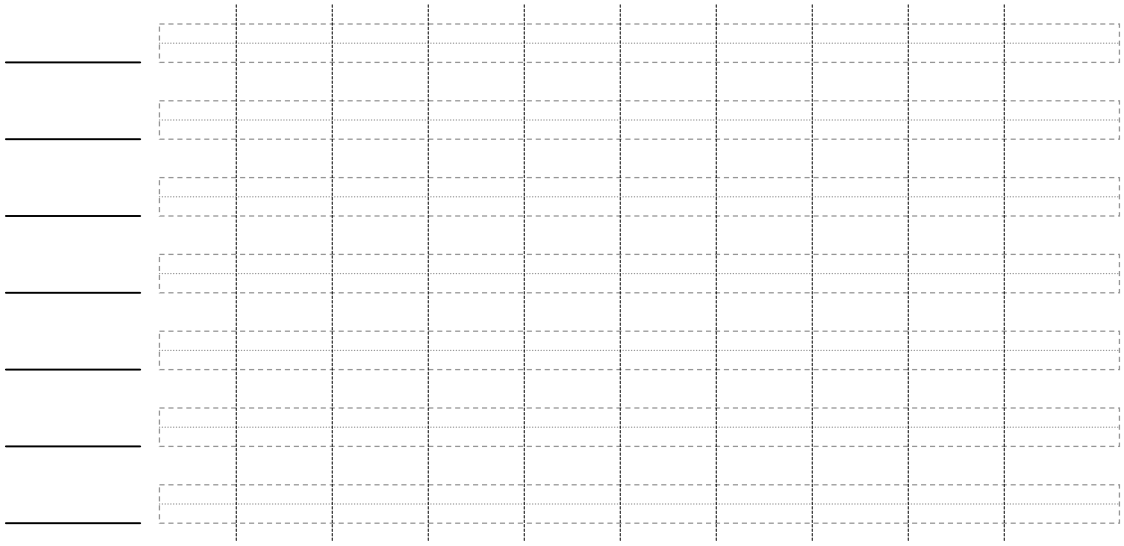
b) How many wait states are involved in each of the two transactions in the diagram?
Transaction 1 (A1-D1):

Transaction 2 (A2-D2):

c) For each transaction, indicate whether the *master* or *slave* is driving the data signals:
Transaction 1 (D1):

Transaction 2 (D2):

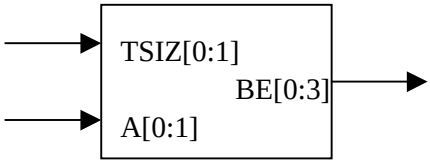
d) Draw a timing diagram for a 4-word burst transfer. Refer to part (a) for acceptable format for the timing diagram. Do *not* show arbitration signals or the MPC823 signals that relate only to burst accesses (i.e., BURST*, BDIP*, and BI*). As long as you indicate a reasonable burst transaction, you need not follow the MPC823 burst protocol exactly.



e) List one advantage and one disadvantage of burst transfers.

8. For this problem, you will design a simple SRAM-based memory system for the MPC823. Refer to the problem 9a for an MPC823 bus timing diagram.

a) Your first task is to design a module that takes the transaction size control signals and the low-order address bits and generates **high-true** byte enables. The logic symbol for the module and the definition of the transaction-size signals TSIZ[0:1] are given below. Follow the PowerPC convention that bit 0 is the most significant bit of each bus. Complete the truth table.



TSIZ[0:1]	Access Size
00	Word
01	Byte
10	Halfword
11	Unused

TSIZ0	TSIZ1	A0	A1	BE0	BE1	BE2	BE3
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	X	X	X	X	X	X

b) Draw the logic symbol for a standard 8Kx8 SRAM device. Clearly indicate the width of all busses.

c) Using your module from part (a), 8Kx8 SRAMs from part (b), and standard logic gates as needed, build a 64 Kbyte memory for the MPC823 occupying a contiguous region of address space starting at address 0x00180000.

d) Given the following delay values, compute the delay for a read to your memory (from the first clock edge where the MPC823 outputs are valid to valid data on the data bus). You must show all your work (i.e., the full process of deriving your value) for full credit.

SRAM read data valid from address valid	30 ns
SRAM read data valid from CS* asserted	35 ns
SRAM read data valid from OE* asserted	10 ns
Arbitrary 4-input logic gate delay	4 ns

e) The MPC823 requires 6 ns of setup time before a clock edge on its inputs, including the data bus. How many wait states are required for reads to this memory if the bus clock is 40 MHz? Again, show all your work for full credit.

f) How would your byte-enable module from part (a) change if the data bus was 64 bits wide instead of 32 bits wide? Assume that the unused TSIZ code of '11' indicates a 64-bit (doubleword) access. Draw the new logic symbol and describe how the internal logic would change. You don't need to do a full truth table.

9. Nate's question