READ AND FOLLOW THESE INSTRUCTIONS.

- Do not begin until you are told to do so.
- You have two hours; budget your time. The questions are not of equal weight; do not spend too much time on a question that is not worth many points.
- Read through all of the questions before starting to work.
- Make your answers brief and to the point. Long, rambling responses that attempt to cover every possibility will be penalized. We reserve the right to grade only the first 25 words of your answer.
- This exam is **closed notes**. You may use the MPC823 data book, the "PowerPC Programming Pocket Book", and/or a printout of Appendix F from the green book as reference material. You may *not* share reference materials with other students.

Name: _____

I have neither given nor received aid on this exam, nor have I concealed any violation of the Honor Code.

Signature: _____

Pages	Questions	Points	Score
2	1-3	48	
3	4-6	50	
4	7-9	30	
5	10-11	38	
6	12	24	
7-9	13	80	
10-11	14	60	
12	15	30	
13-14	16	40	
15	17-18 (EC)	10	
	Total	400	

1. (16 pts.) Name two common embedded-system design constraints *other than cost* not shared with general-purpose computers. For each constraint, give an example of a system for which that constraint is likely the most critical one.

2. (14 pts.) For each of the following descriptions, list **all** the memory types that fit. You may use the same type more than once. Choose from: SRAM, DRAM, ROM, PROM, BBSRAM, EPROM, EEPROM, Flash.

   a. High density (one transistor per bit)

   b. Non-volatile, contents can be updated one byte at a time

   c. Very fast read and write access times, suitable for caches

   d. Might actually be a UV EPROM in a windowless package

   e. Widely used for field-upgradable, non-volatile program storage

3. (18 pts.) For each of the three interrupt structures listed below, indicate how interrupting devices are identified and prioritized.

type	identified	prioritized
non-vectored		
vectored		
autovectored		

4. (20 pts.) Consider a 3-bit analog-to-digital converter with Vref = 8 V. The absolute **and** differential non-linearities are specified on the data sheet as ± 1/4 LSB. You observe that the output transition from 2 to 3 occurs at an input voltage of 3.25 V. What is the range in which the 3 to 4 transition should occur?

5. (10 pts.) Define *bus parking*. What is its purpose?

6. In the MPC823 bus arbitration scheme, a bus master deasserts $\overline{\text{BR}}$ as soon as it starts its transaction.

   a. (6 pts.) What prevents the next bus master from starting its transaction before the previous master's transaction is finished?

   b. (10 pts.) If we modified the arbitration protocol so that the current master continued to assert $\overline{\text{BR}}$ until it completed its transaction, then the next master could start its transaction as soon as its $\overline{\text{BG}}$ is asserted. Give the primary disadvantage of this modification. (Hint: there's a good reason the MPC823 doesn't do this.)

   c. (4 pts.) What would be the primary advantage of the modification in part (b)?

7. (12 pts.) Consider a bus master that initiates a read transaction. For each bus type, describe briefly but precisely *when* the master samples the slave's data from the bus.

   a. synchronous

   b. semi-synchronous

   c. asynchronous

8. (10 pts.) What common characteristic of bus protocols is exploited by both pipelined and multiplexed busses? How do these two approaches use this characteristic to achieve opposite goals?

9. (8 pts.) What is the main advantage of a split-transaction bus over a pipelined bus?

10. DMA I/O transfers to and from disks are done in large blocks, e.g. 4096 bytes at a time.

    a. (6 pts.) What advanced bus feature, supported by the MPC823, improves the efficiency of these transfers?

    For parts (b)-(d), give the number of bus transactions *and* minimum number of bus clock cycles required to transfer 4096 bytes from a DMA disk device to memory.

    b. (6 pts.) Using DMA *with* feature from part (a)

    c. (6 pts.) Using DMA *without* feature from part (a)

    d. (6 pts.) Not using DMA

    e. (6 pts.) What is the term for non-DMA I/O transfers (as in part (d))?

11. (8 pts.) List one advantage and one disadvantage of using a separate DMA controller compared to an I/O device with built-in DMA capability.

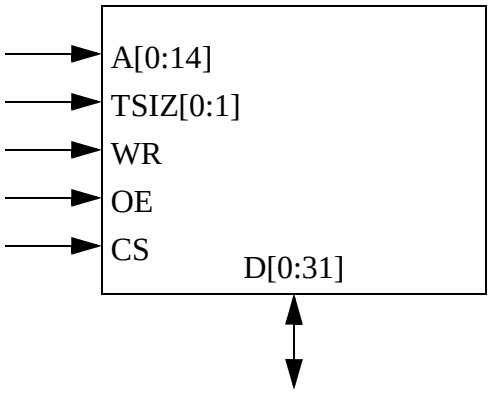
12. (24 pts.) Write the PowerPC assembly-language equivalent of the following C code. Use the ABI discussed in class.

```
int func1(int a)
{
	return func2(a, a + 10);
}

int func2(int b, int c)
{
	return b + c;
}
```

13. Memory system design.

a. (20 pts.) Using the parts listed on the data sheet handout, plus any logic gate with three or fewer inputs, build a 32 Kbyte memory module that has the following block diagram:



b. (15 pts.) Show the logic required to connect the module from part (a) to the MPC823 bus starting at address 0x02500000 with exactly one shadow location. Again, use only logic gates with three or fewer inputs. Do not worry about generating $\overline{TA}$.

c. (15 pts.) Calculate the read and write access delays for your memory in part (b), i.e., from the start of a bus transaction to the completion of the access at the SRAM. Assume that the bus clock is 50 MHz, and that logic gates have a delay of 4 ns.

d. (10 pts.) If the MPC823 requires 10 ns of setup time on the data bus, how many wait states will you need for read transactions? How many for write transactions?

e. (20 pts.) Consider how you would use one or more instances of the memory module from part (a) to build a 128 Kbyte (32Kx32) memory that *efficiently* supports four-word burst transfers. Sketch your design at a very high level, using **only** these components: your memory modules, an address decoder, and a control module. Show connections to the MPC823 bus signals on the left. **Label all inputs and outputs of each component clearly and precisely.** You do not need to design the address decoder or control module; just show their inputs and outputs.

A[6:31] ———

RD/$\overline{\text{WR}}$ ———

$\overline{\text{TS}}$ ———

$\overline{\text{BURST}}$ ———

$\overline{\text{TA}}$ ———

In questions 14-16, you will build an answering machine using the MPC823 and other parts specified on the data sheet handout. Your answering machine should answer the phone, sample incoming messages at 40 kHz, store them, and play them back when the user presses the Play button. If the user presses the Erase button while a message is playing, that message will be erased. The machine should handle up to 4 messages with a maximum message length of 30 seconds. Minimize the cost of your design.

A high-level block diagram is given for you on the data-sheet handout. Question 14 asks you to design some of the components. Question 15 deals with the memory system. Question 16 asks you to do a high-level design of the required software. Note that these questions are independent, so if you get stuck on one you can move ahead to another.

14. For this question, basic bus-interface logic (generation of chip selects, OE, $\overline{\text{TA}}$, etc.) may be shown as a single module (you don't need to design it). Assume that a 1 MHz clock signal is available.

    a. (15 pts.) Use one of the given timers (not an MPC823 internal timer) to generate periodic interrupts at a rate of 40 kHz (labeled "40 kHz Interrupt Generator" on the diagram). List all timer register values and show how you would connect the timer to the MPC823.

    b. (20 pts.) To enforce the maximum message length, build a watchdog timer that generates an interrupt after 30 seconds (labeled "30-second Timeout Generator" on the diagram). Show all hardware connections and register values.

c. (10 pts.) Which of the listed analog-to-digital converters will you use? Why? Show your work.

d. (15 pts.) Using your chosen ADC device plus other components, build a conversion module (the "ADC Unit") that will *independently* generate digital samples at a 40 kHz rate without any processor involvement. The module should have an output that generates an interrupt only when each conversion is complete. Show all hardware connections and register values.

15. Answering-machine memory system. See discussion at top of page 10.

    a. (10 pts.) How much memory will your system require to store messages?

    b. (10 pts.) Which two types of memory might be appropriate for this system, and why? Choose one of the two types for your system, and give two reasons for choosing it over the other type.

    c. (10 pts.) How might you reduce the machine's memory requirements without reducing the number of messages or message length? What would be the impact of this change?

16. (40 pts.) Anwering-machine software design. See discussion at top of page 10. The block diagram on the data sheet indicates the five interrupts that will be generated in your system, labeled USER, CALL, EOC, TIME, and TIMEOUT. The Play and Erase buttons share a single interrupt (USER), just as your buttons did in Lab 6. The component data sheet also has further details on the operation of the telephone interface module.

    For each interrupt, describe the corresponding ISR's operation using pseudocode or a flowchart.

17. (5 pts. extra credit) What flavors of cookies did we have on the last day of class?

18. (5 pts. extra credit) Give the first and last names of any two TAs this term. Spelling counts!