EECS 373 Exam 2

Fall 2002, Prof. Mark Brehob

Name: _____ UM ID: _____

Unique name: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

_____

I agree not to discuss this exam with anyone other than instructor until noon on Tuesday.

_____

Scores:

#	Points
I	/10
II	/25
III	/15
IV	/30
V	/20
Total	**/100**

NOTES:

- Closed notes. White book and ABI only!
- Don't spend too much time on any one problem.
- You have 90 minutes for the exam.

I. Interrupts (10 points)

1) Identify the following as synchronous (**S)** or asynchronous (**A**) interrupts. (**5 points, -2 per wrong answer, min 0**)

   - Page fault
   - Real time clock interrupt
   - Timer capture interrupt
   - Divide by zero
   - Illegal instruction
   - Interrupt generated by the A to D converter

2) If SIPEND has the value 0x03040000 and no interrupts are masked out, what value would be in SIVEC if it were read as a byte? Give you answer in hex. **(5 points)**

II. Timers (**25 points**)

For these problems, assume the system clock frequency of the MPC823 is 25Mhz exactly.

1. Say you want to have Timer 1 generate an interrupt every 10ms. You wish to choose settings to that insure the following:
   - The interrupts occur exactly every 10ms
   - The value in TCN1 is as small as possible when the interrupt is generated.

   a) What value will be in TCN1 when the interrupt is generated? (**5 points**)

   b) Show the settings for TMR1, TGCR, TRR1 at the moment when the counter first starts counting. Give all answers in hex and be sure that you have given values for every bit in each of the registers. If you thing a given bit doesn't matter, then set it to zero. You may assume other registers are set as needed. (**12 points**)

      TMR1 =

      TGCR =

      TRR1 =

2. Write assembly code that clears a capture interrupt set by TMR2. It should not clear any other interrupt. You may assume the value of (IMMR &0xFFFF0000) is in register 3. (**8 points**)

III. Clock division (**15 points)**

Using a standard counter, with a synchronous and a D or T flip-flop design a circuit that takes a 140 MHz clock that has a duty cycle of 25% and outputs a 10MHz clock with a duty cycle of 50%.

IV. Error correction and detection. (30 points)

1. Consider the following encoding scheme which uses 6 bits (A,B,W,X,Y,Z). A and B are data bits. The parity groups are as follows: W={A}, X={B}, Y={A,B}, Z={A,B}. We are using even 1's parity. Assume are correcting one-bit errors using this encoding and trying to detect larger bit-errors when possible. For each of the following encodings do one of the following:

    - Identify the encoding as legal (write the word **legal**.)
    - Identify and fix a one-bit error (write the corrected 6-bit pattern)
    - State that a bit error of greater than 1 bit occurred (write the word **error.)**

In all cases the order is AB WXYZ. (**3 points each)**

`00 0001` _____

`11 1100` _____

`01 0011` _____

`11 1101` _____

`10 0001` _____

2. Using the Veterbi algorithm, show how the following data stream would be corrected. Assume that we are still using even parity! Show your work in the following table. **(15 points)**

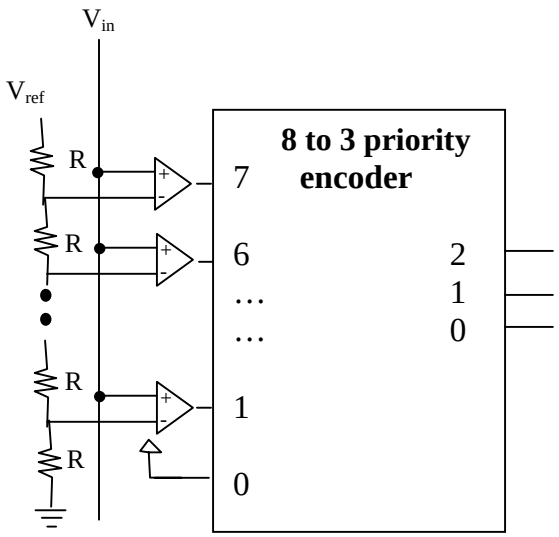
Data	0	0	1	0	1
Parity	0	1	0	1	1

	Step1		**Step2**		**Step 3**		**Step 4**		**Step 5**	
Received										
	path	cost	path	cost	path	cost	path	cost	path	cost
Node0										
Node1										
Node2										
Node3										

Actual **data** sent (according to the algorithm): _____

V. Analog to Digital Conversion and Bus Interfacing Questions (20 points)

Consider the hypothetical 3-bit A to D converter: the ADC0505. The diagram of the Flash ADC follows. Assume Vref is 4 volts, and that there are actually 8 resistors, each with a value of R.



1. What is the maximum quantization error that could occur when converting from analog to digital? **(4 points)**
   a. In units of LSBs?

   b. In units of Volts?

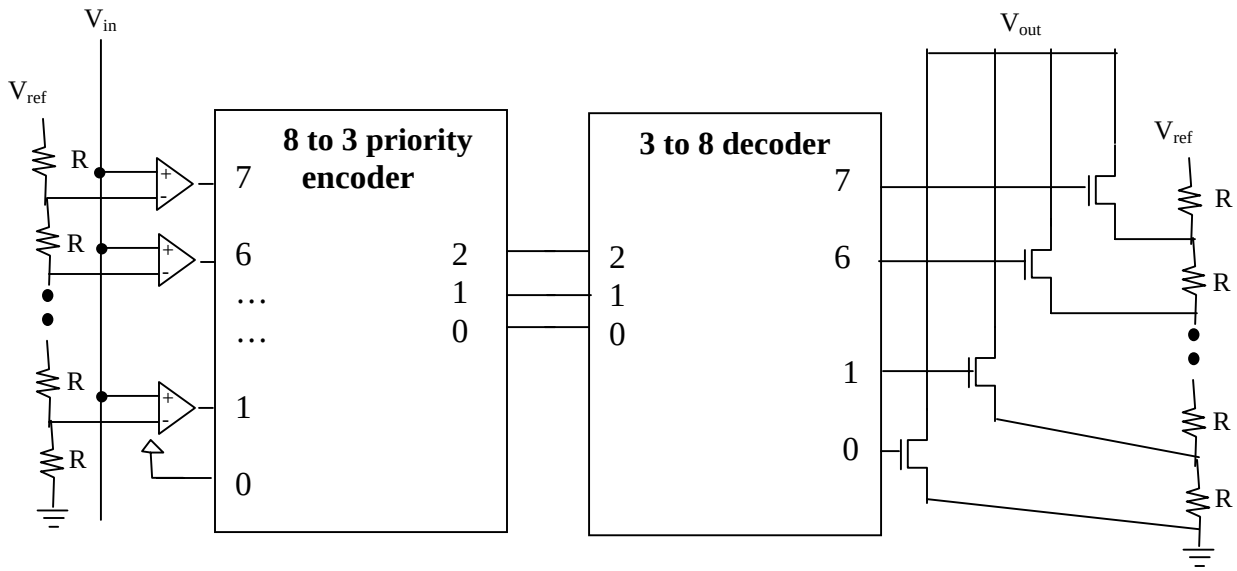
2. Assuming just the effects of quantization error, what voltage interval converts to the value 5 decimal? **(3 points)**

3. Consider what would happen if the following DAC were connected to the output of the Flash ADC as shown. Again, assume that the resister latter has a total of 8 resistors. If everything were ideal, what would be the output (V_{out}), in volts, if the value for V_{in} were: **(6 points)**

    a. 3.2 volts _____

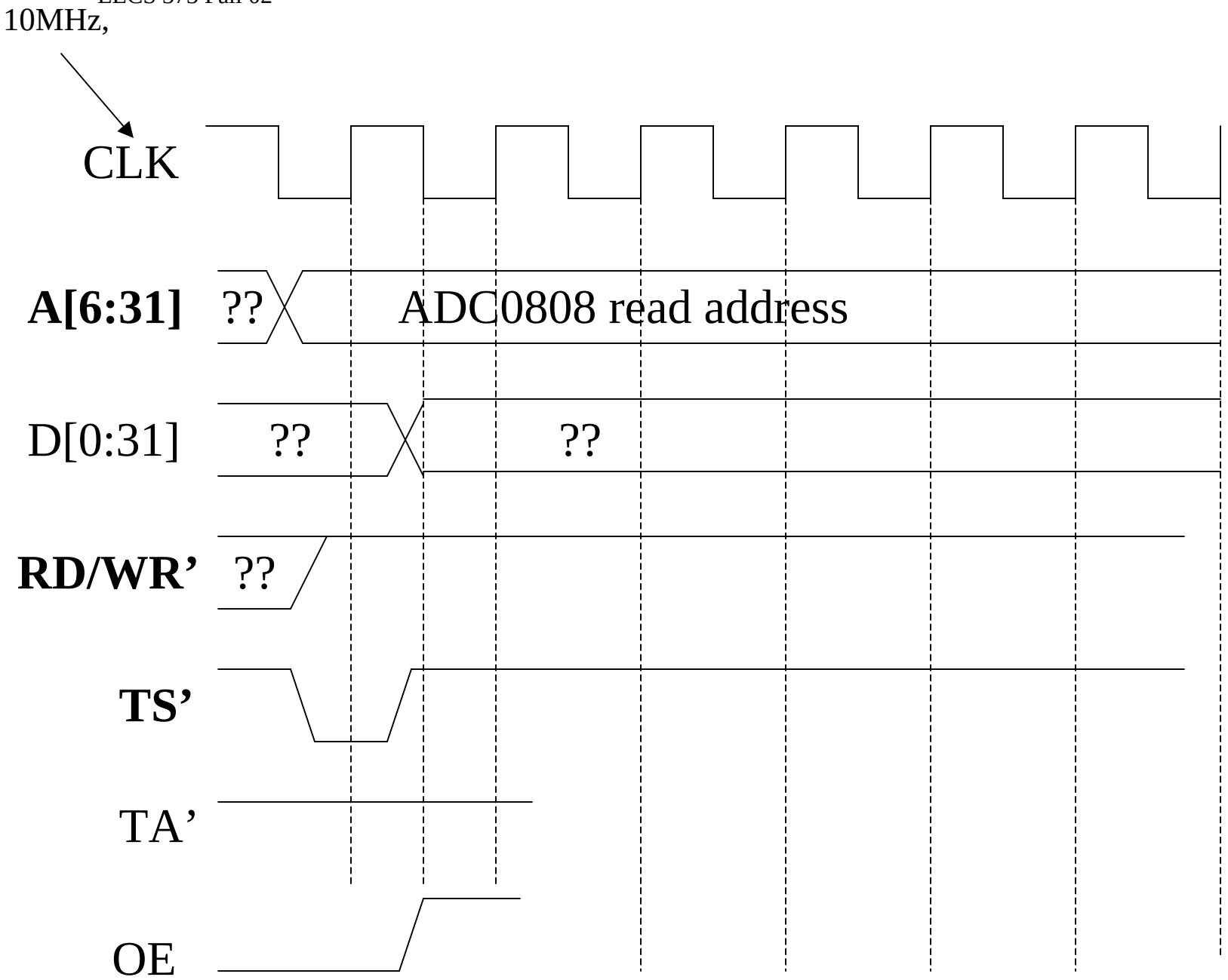
    b. 1.6 volts _____

    c. 1.8 volts _____



The ADC0505 provides output data with a tri-state output latch like theADC0808 used in lab. The signal used to enable or output data from the tri-state latch is OE. Data is guaranteed to be stable after asserting OE by no more then 300ns. Assuming that OE is decoded from the address bus and is stable as shown in the following figure (at the falling edge of the clock.) Assume the clock has a 10MHz frequency with a a duty cycle of 50%.

4. Complete the drawing of the read cycle for OE and TA with no more wait states then required. *Clearly label which bus cycles are wait states.* **(7 points)**


10MHz,
CLK
A[6:31]
??
ADC0808 read address
D[0:31]
??
??
RD/WR’
??
TS’
TA’
OE