EECS 427: VLSI Design I
Fall 2008 Syllabus, Revised 8/23/08

Texts: Default = Rabaey, WH = Weste and Harris, CBF = Chandrakasan, Bowhill, and Fox

Date	**Topic**	**Reading/Coverage**	**Notes, assignments due**
September 2	Course Introduction, Manufacturing	1.1-1.3 (review), 2.2, WH 3.2	CAD tutorial, 9/2 5:30-7:30pm & 7:30-9:30, 1695 CSE
9/4	Design Rules & Layout	2.3, Insert A, WH 1.5, WH 3.3	CAD1 due 9/8
9/9	Design Styles Overview	8.1-8.4	
9/11	CMOS Review	5.4, 6.2	HW1 due in class CAD2 due 9/15
9/16	Interconnect Review	4.3.1, 4.3.2, 4.4.1-4.4.3, 9.3.3	HW2 due in class (teams)
9/18	Project Architecture and Intro to Logical Effort	handouts	
9/23	Logical Effort	handouts	
9/25	Adders	11.1-11.3.1	CAD3 due 9/26
9/30	Adders	11.3.2-11.3.3	
October 2	Shifters	11.5, WH 10.8	HW3 due in class (initial proposal)
10/7	Multipliers	11.4	
10/9	Power/Energy, Dynamic Logic	5.5, 6.3, CBF Ch. 7	CAD4 due 10/10
10/14	Low-Power ALUs	11.7	
10/16	Quiz 1		
10/20, 10/21 - Fall Study Break, No Classes			
10/23	Counters, pipelining	WH 10.5, notes	CAD5 due 10/24
10/28	Synthesis/APR flow	Notes, WH 8.4	
10/30	Timing, skew/jitter	10.1-10.3	CAD6 due 10/31
November 4	Timing cont., D-Q, pulsed latches	10.3, 7.4	HW4 due in class (detailed proposal)
11/6	Design-for-Test (DFT)	Insert H.3, CBF Ch. 25	CAD7 due 11/7
11/11	Memory Core and Peripherals	12.1-12.3	
11/13	Memory Reliability and Power	12.4, 12.5	CAD8 due 11/14
11/18	System-Level Power Reduction	6.4.2, CBF Ch. 4	
11/20	Quiz 2		
11/25	Clock Distribution & Robustness	10.3.3, 10.6, CBF Ch. 13	
11/26, 11/27, 11/28 - Thanksgiving Break, No Classes			
December 2	Advanced Interconnect Techniques	9.5	
12/4	Power Grid and Other Issues	WH 12.3, CBF Ch. 24	
12/9	Process Variation		Course Evaluations in class
12/12	Final Project Demos Final Project Presentations (Time TBD)		CAD9: Final Due HW5: Final Report due @7am HW6: Presentations

Summary of *tentative* due dates:

HW1 (problem set): Thursday, Sept. 11 in class
HW2 (teams): Tuesday, Sept. 16 in class
HW3 (initial proposal): Tuesday, Oct. 2 in class
HW4 (detailed proposal): Tuesday, Nov. 4 in class
HW5 (final report): Friday, Dec. 12 at 7am
HW6 (project presentations): Friday, Dec. 12 (Time TBD)

All CADs due at 7pm except CAD9.
CAD1 (inverter/nand/mux): Monday, Sept. 8 (1 week)
CAD2 (D flip-flop): Monday, Sept. 15 (1 week)
CAD3 (register file): Friday, Sept. 26 (1+ week)
CAD4 (ALU): Friday, Oct. 10 (2 weeks)
CAD5 (shifter): Friday, Oct. 24 (2 weeks)
CAD6 (program counter): Friday, Oct. 31 (1 week)
CAD7 (datapath): Friday, Nov. 7 (1 week)
CAD8 (controller): Friday, Nov. 14 (1 week)
CAD9 (project completion/demo): Friday, Dec. 12 (4 weeks)