MichiganEngineering

EECS 427
Discussion 1

Tuesday, September 9, 2008

Administrative Stuff

- CAD1 due yesterday
- Homework 1 due Thursday, beginning of lecture
- Homework 2 due week from today – Sept. 16
  - Due at beginning of Tuesday's lecture
  - List of group members (groups typically 3-4 people)
- CAD2 due next Monday, Sept. 15
  - CAD2 again an individual assignment
  - CAD3 and on – group assignments
- Out of town again this weekend (conference)
  - Extra office hours – Friday, Sept. 12 1-3pm
  - Will be available by email again
- No discussion next Tuesday – instead, CAD3 discussed on Friday?

Questions regarding CAD1?

??

Layout Tips & Tricks

- Creating a hierarchical layout
  - Don’t have to copy & paste geometries!
  - Instantiate previous layouts using ***Create->Instance*** (Shortcut: i)
- Viewing hierarchy
  - Two ways to change number hierarchy display on screen.
    - Through Menu
      - Options -> Display…
      - Change the Display levels
    - Through Hot Key
      - Shift+f: show all hierarchy
      - Ctrl+f: hide all hierarchy

Layout Tips & Tricks (cont'd)

- Editing in hierarchy
  - Can open up layout using *Library Manager* (saved changes will be reflected after redraw – Ctrl+r)
  - Can go to ***Design->Hierarchy->Descend*** (Shortcut: X)
    - Opens up design in current window
    - Return to previous level in hierarchy: ***Design-> Hierarchy->Return*** (Shortcut: B)
- Adding geometries
  - Rectangle -> r
  - Path -> p
  - Label -> l

Layout Tips & Tricks (cont'd)

- Modifying geometries
  - Copy -> c
  - Move -> m (whole shape only)
  - Stretch -> s (whole shape or edge)
  - Chop -> C
  - Merge -> M
- Rotating and Flipping
  - After selecting copy , move, create instance, etc., HIT F3!

**** Hitting F3 in any mode will pop-up the associated form****

- Other useful commands
  - Properties -> q
  - Search -> S
  - Select all -> Ctrl+a
  - Deselect all -> Ctrl+d

LSW Management

- By default, LSW window shows TONS of layers!!
- You can set the LSW to show only the layers that are in your layouts
  - [In Virtuoso Window] ***IBM_PDK->LSW->Present Layers Only***
- To add more layers that are not in the LSW
  - [In LSW Window] ***Edit->Set Valid Layers***

Gravity

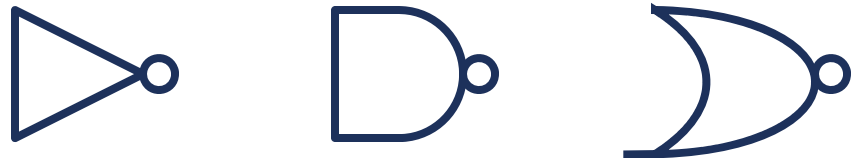
- One of the functions that is turned off by default is gravity
  - **THANK GOODNESS!!**
- Gravity allows you to lock on to an edge or corner of a shape when your mouse cursor get close
  - Annoying or helpful…you be the judge!!
- To turn it on or turn it off.
  - ***Options->Layout Editor*** (Shortcut: E) in Layout view
  - Click on “Gravity On” to toggle between the on and off mode
  - Can also toggle on and off using shortcut: ‘g’

Hierarchical Design

- Make sure you use hierarchical design from now on!!
  - Will make life a whole lot easier

Circuit Design

- General Flow for any design
  - Schematic Creation (how is this circuit supposed to function?)
  - Symbol Generation (more specific symbols useful in hierarchy)



  - Digital Logic Simulation (does it function as expected?)
  - Analog Simulation Testbench Creation (does spice backup digital simulation?)
  - Layout
    - DRC
    - LVS
    - PEX -> parasitic extraction
  - Backannotation and Spice simulation (how does circuit behave with all of parasitics?)

Circuit Design (cont'd)

- We're not done…

ITERATE!!!!!

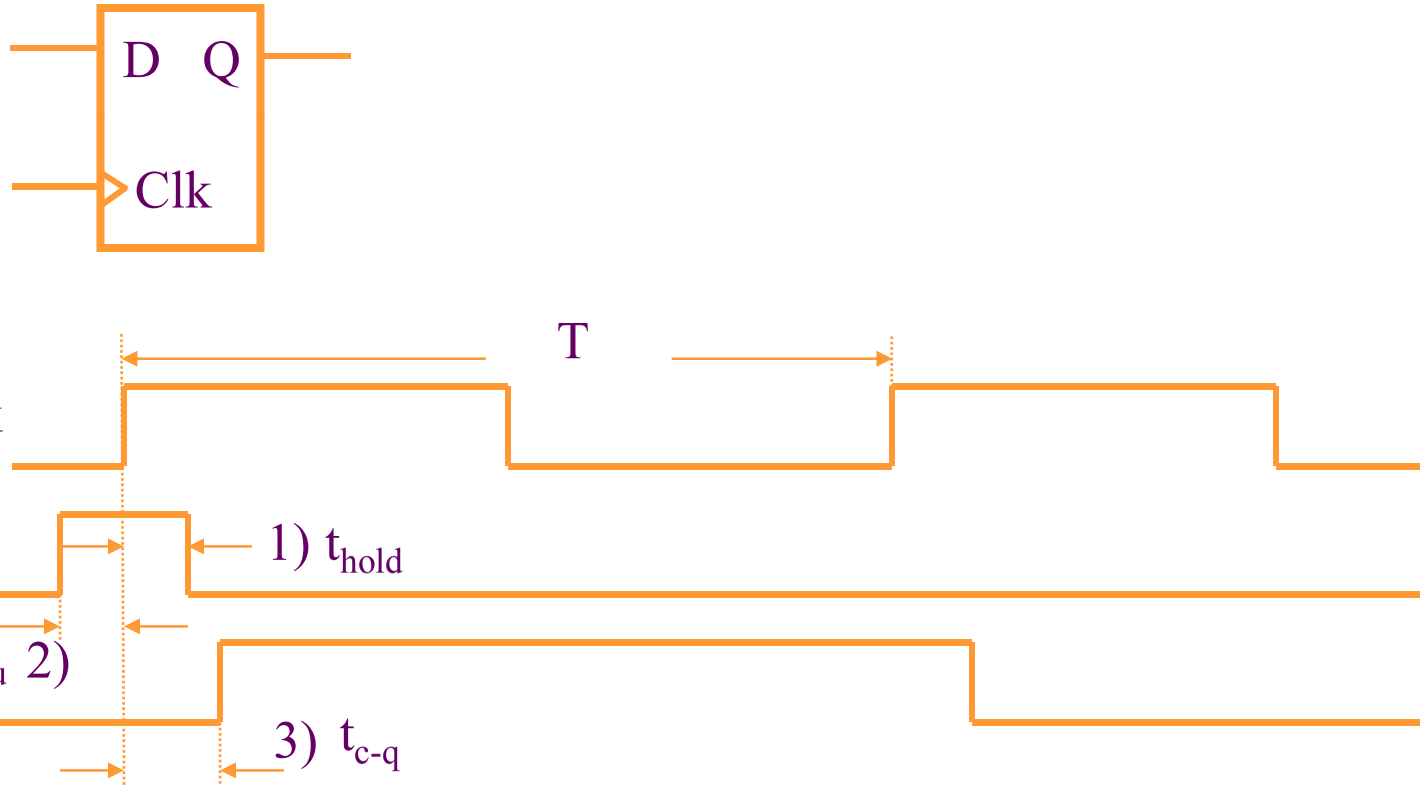
- Modify and possibly redesign to hit specifications (size up gates to meeting timing, relocate cells to reduce interconnect capacitance, etc.)

Backannotation

- Generally in this class, backannotate to 2 places
  - Digital Simulation (Verilog)
  - Analog Simulation (Spice)
- How do we do this?
  - Already learned analog simulation (“calibre” view generation using PEX)
  - Digital simulation backannotation described in Tutorial 1.5

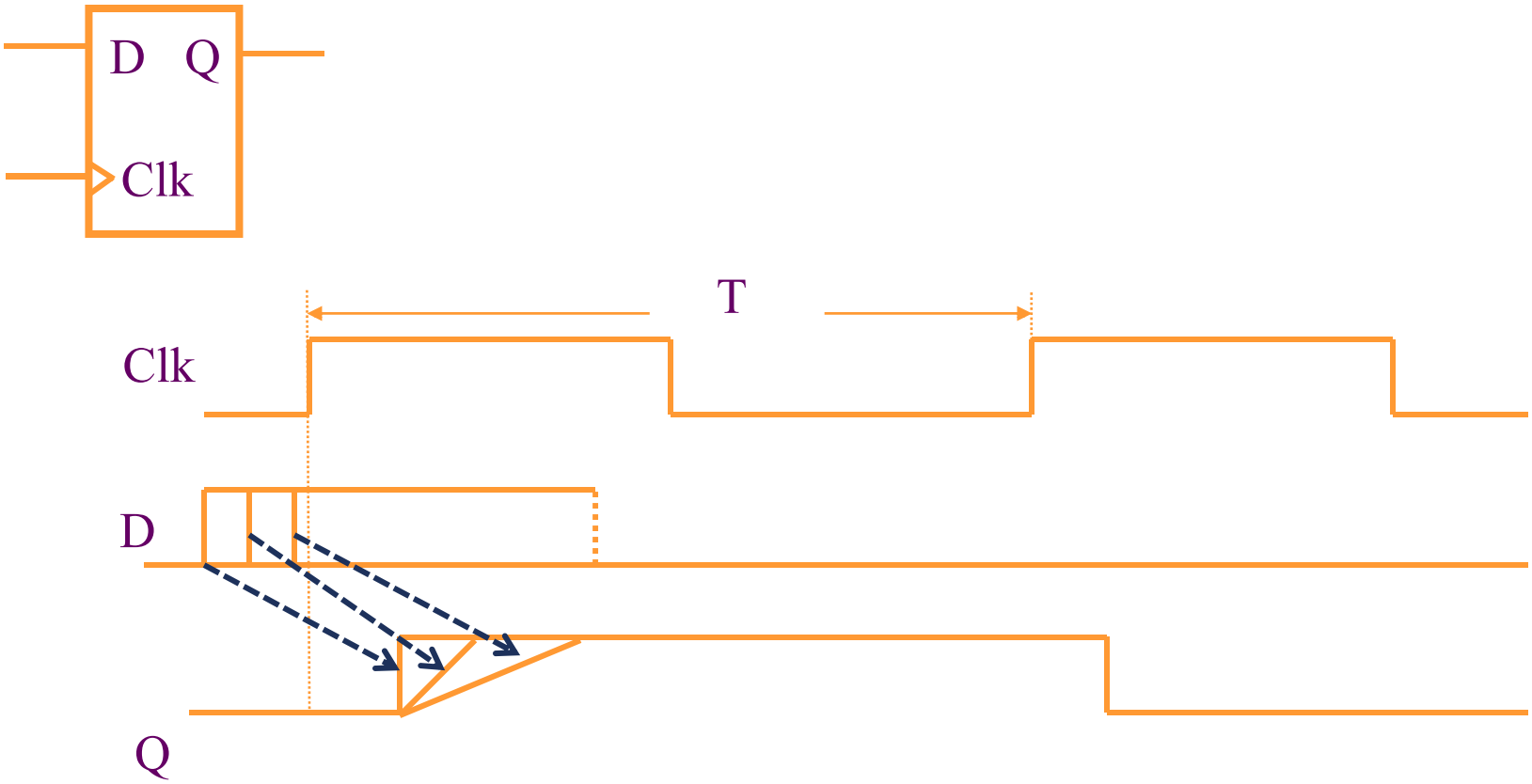
Tutorial 1.5

- Main idea
  - Add Verilog delay property, t_d, to a transistor to represent some delay (e.g., CLK-Q, setup, hold)
  - Use delays to get more accurate representation in simulations
- Review



Tutorial 1.5 (cont'd)

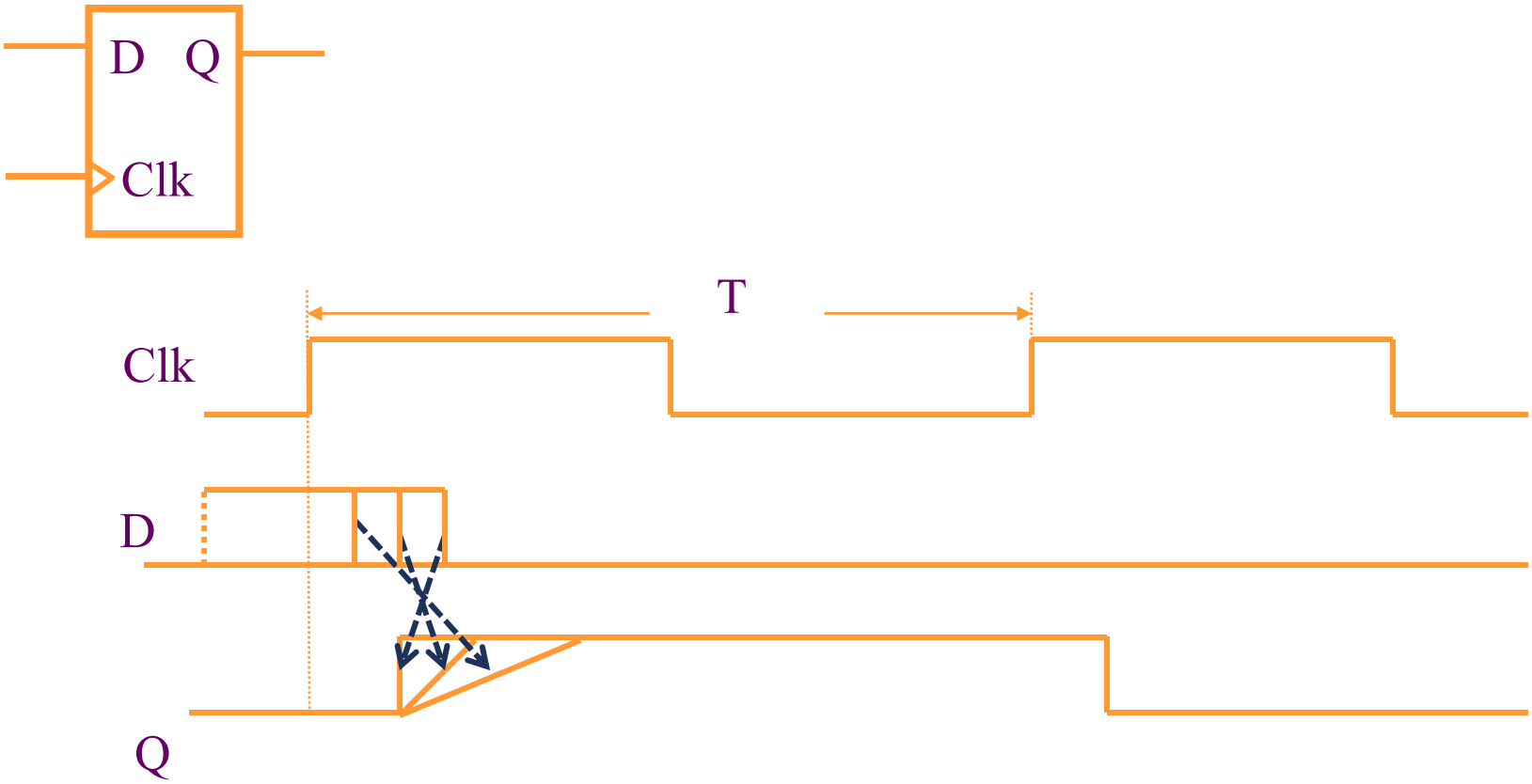
- How do setup and hold affect timing?



- ↓ t_{su} (closer D transitions before Clk, ↑ CLK-Q delay)

Tutorial 1.5 (cont'd)

- How do setup and hold affect timing?



- ↓ t_{hold} (closer D transitions <u>after</u> Clk, ↑ CLK-Q delay)

Tutorial 1.5 (cont'd)

- How to measure setup and hold?
- Setup
  - Store a 1 (0) to the flip-flop and allow to settle for one clock cycle
  - Next clock cycle, change D input >=0.25 clock cycle before rising edge and measure CLK-Q delay (50% CLK -> 50% Q)
  - Run parametric sweep adjusting D transition later and later – closer to rising edge of CLK (make sure hold time is long too, >=0.25 clock cycle, otherwise hold will affect too!!)
  - Setup constraint is time in parametric sweep which causes ≈5% increase in CLK-Q delay (calculated in 2nd step)

Tutorial 1.5 (cont'd)

- How to measure setup and hold?
- Hold
  - Store a 1 (0) to the flip-flop and allow to settle for one clock cycle
  - Next clock cycle, change D input >=0.25 clock cycle after rising edge and measure CLK-Q **(should be similar to 2nd step of setup time)**
  - Run parametric sweep make D transition earlier and earlier (making sure setup time is long, >= 0.25 clock cycle)
  - Hold constraint is time in parametric sweep which causes ≈5% increase in CLK-Q delay (calculated in 2nd step)

Tutorial 1.5 (cont'd)

- Once we characterize setup & hold for cell, backannotate delays into Verilog simulation!!

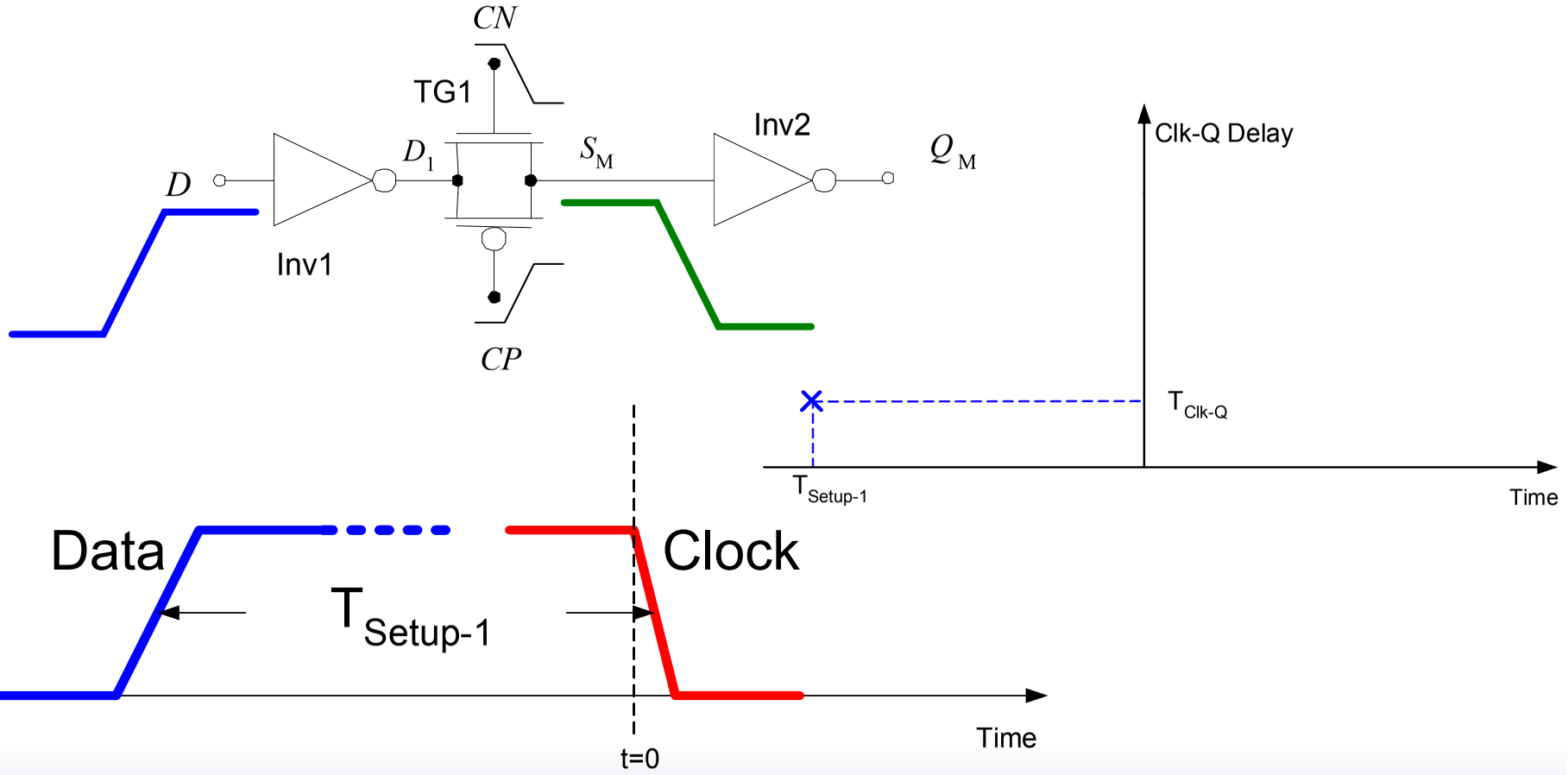
- Further reading – Insert E (pp. 431 – 433)

DONE!!!

Supplemental Slides

Setup/Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



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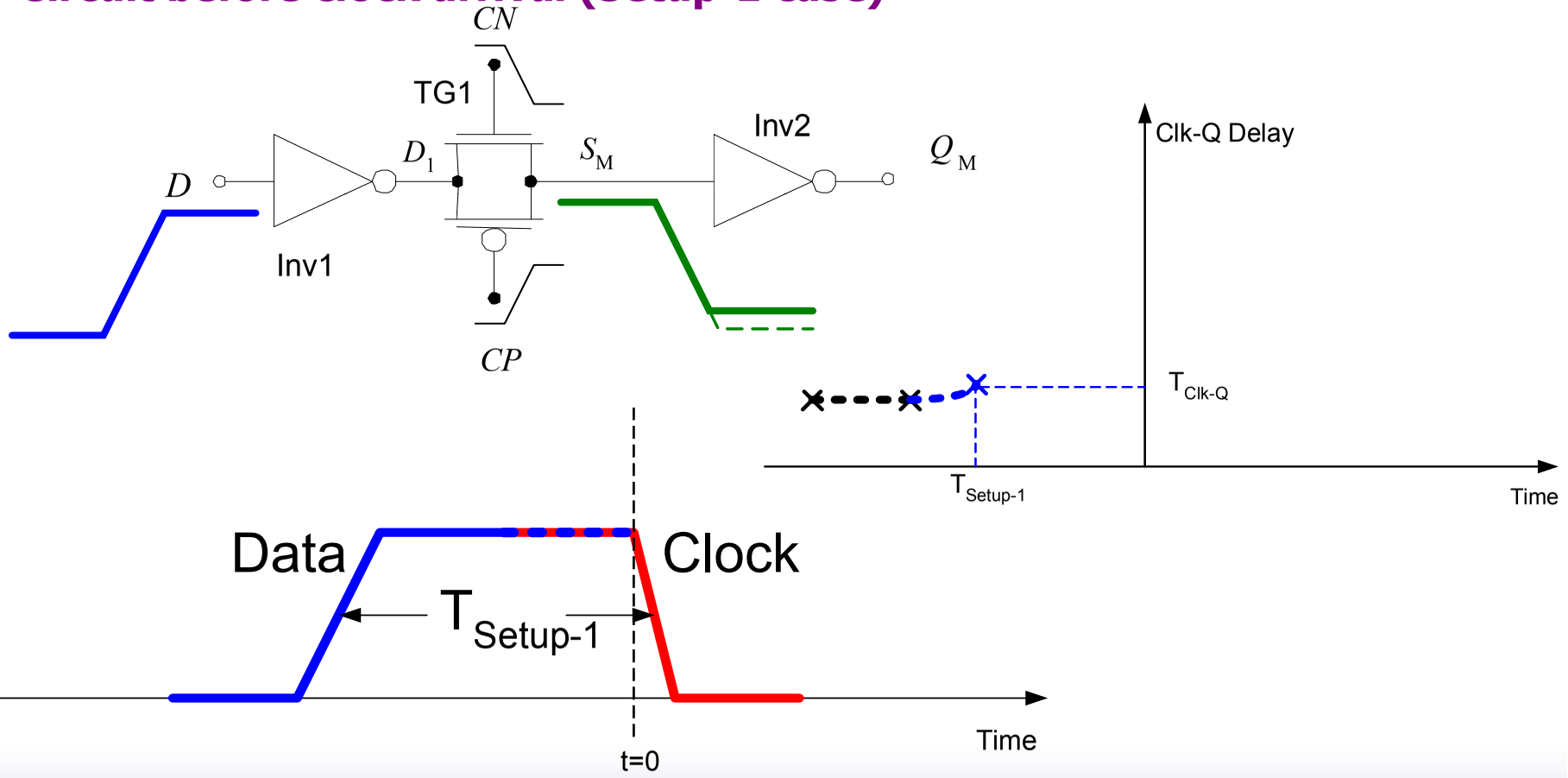

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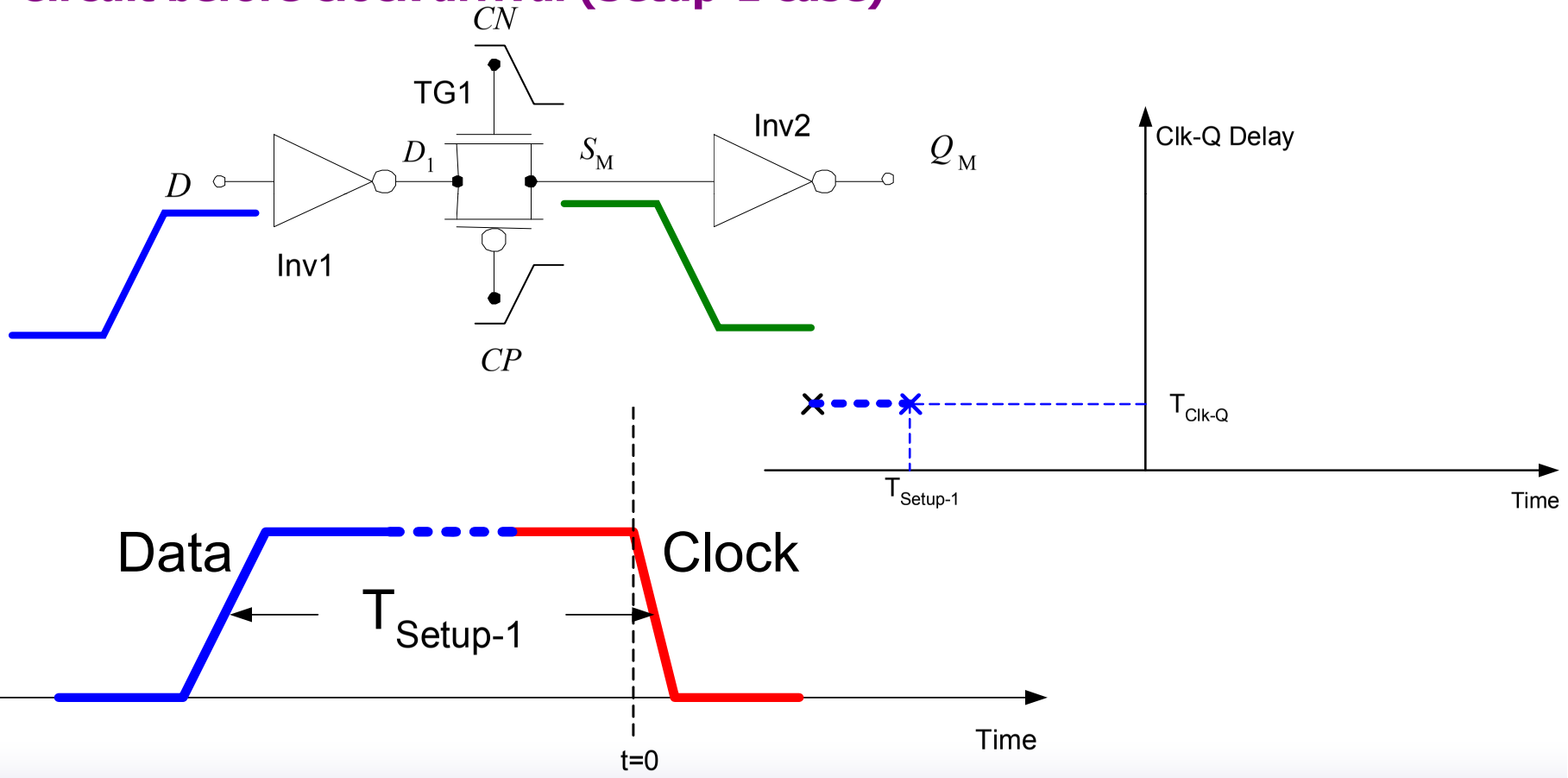

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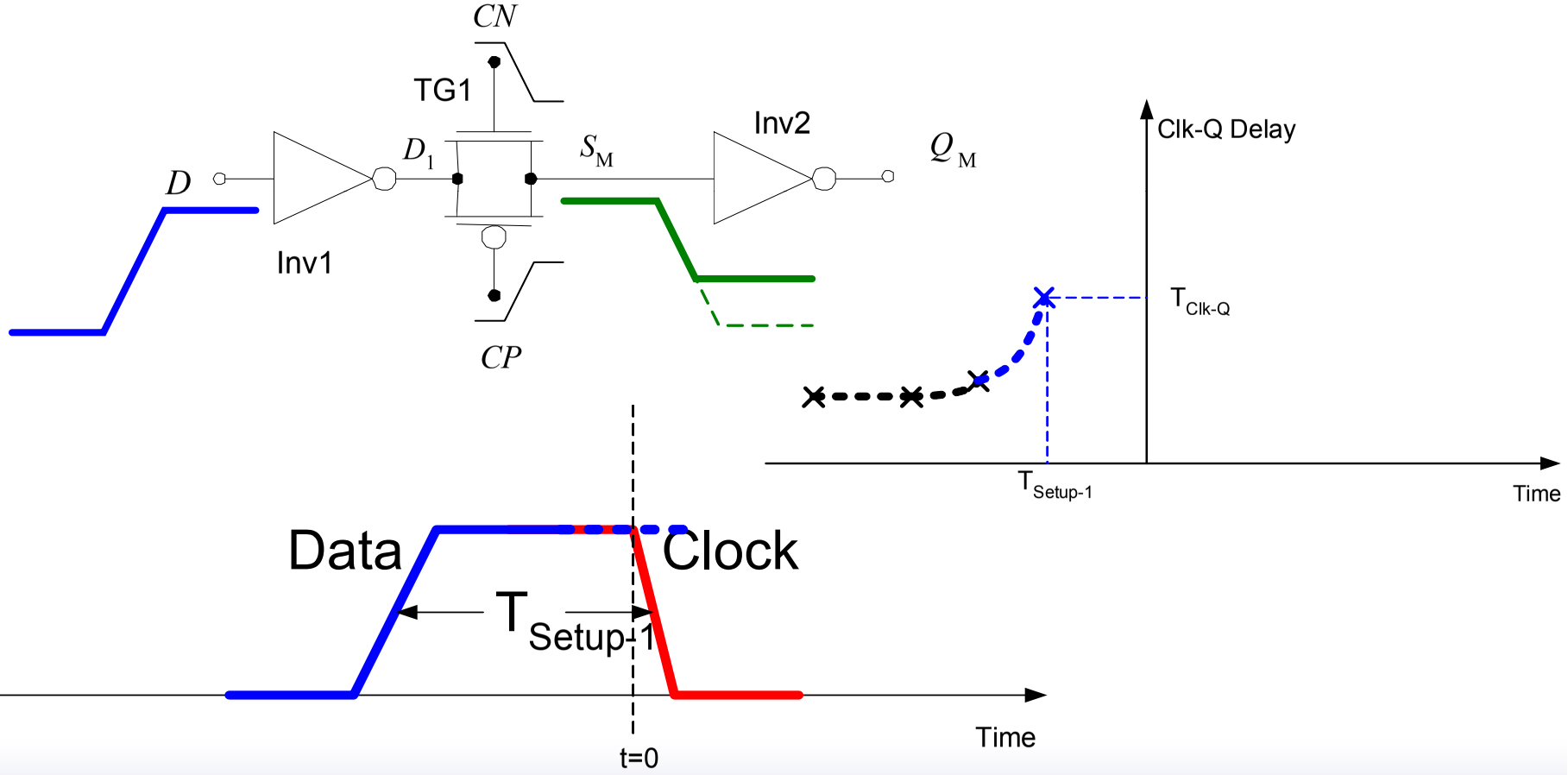

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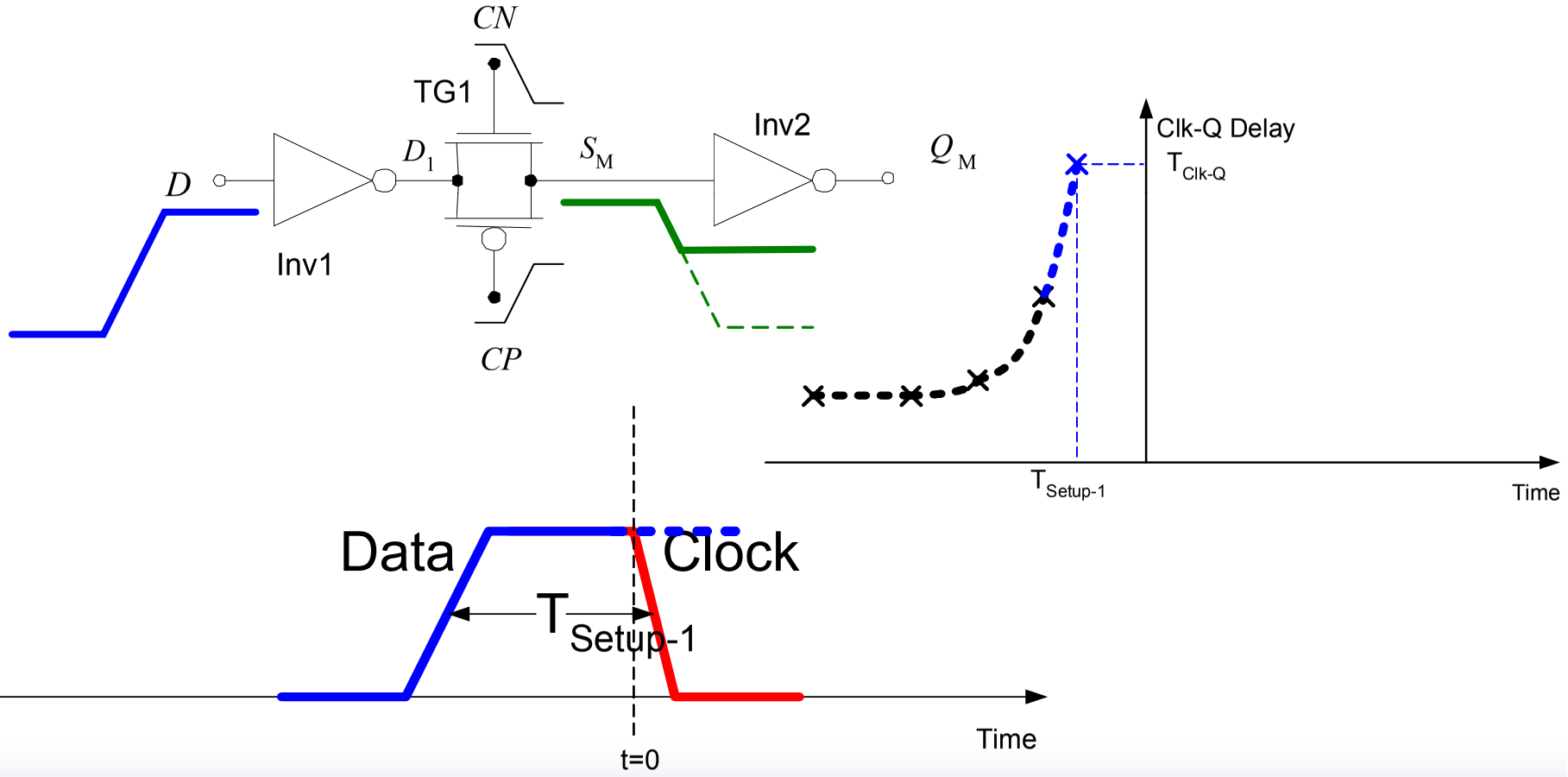

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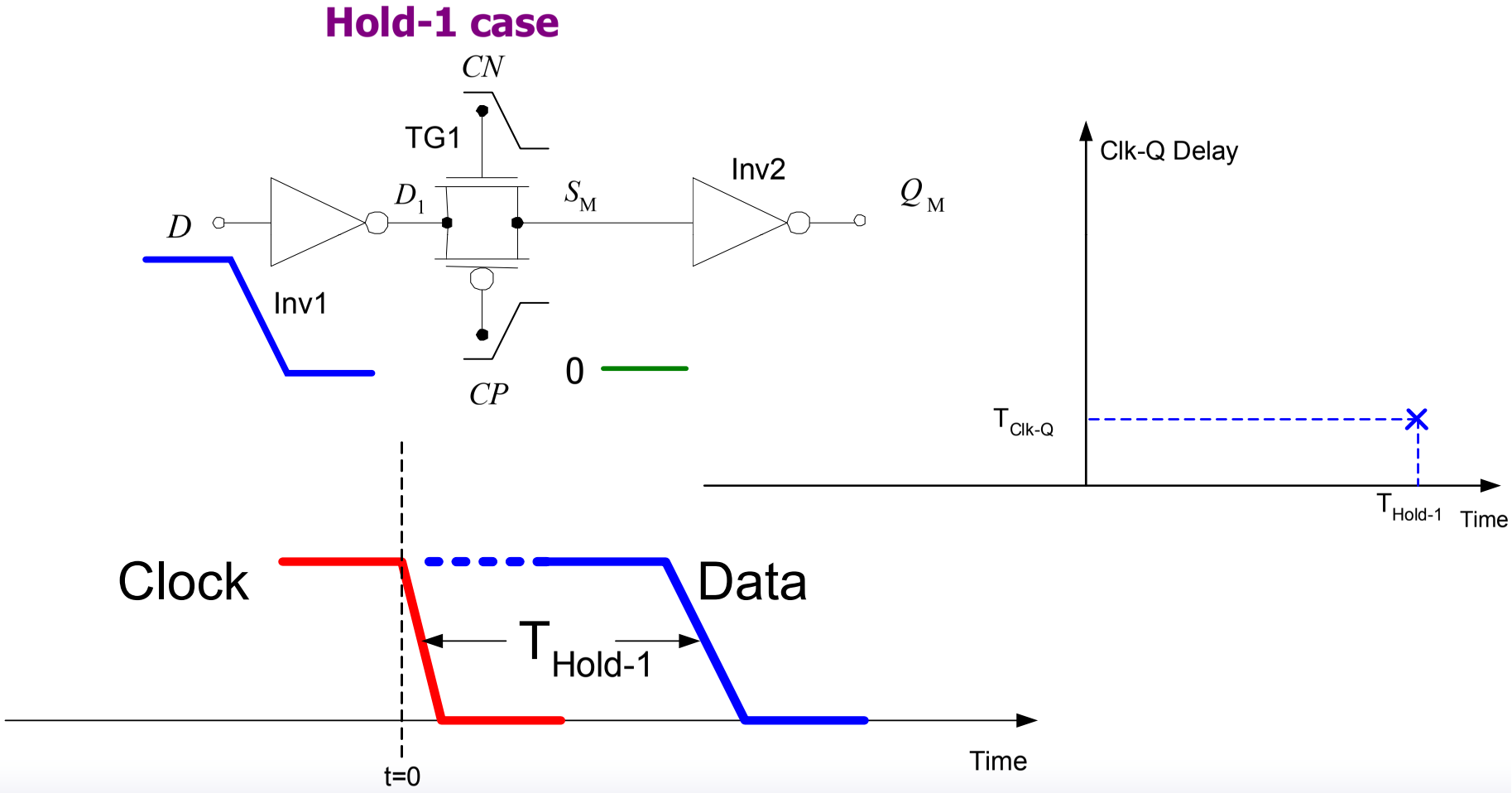

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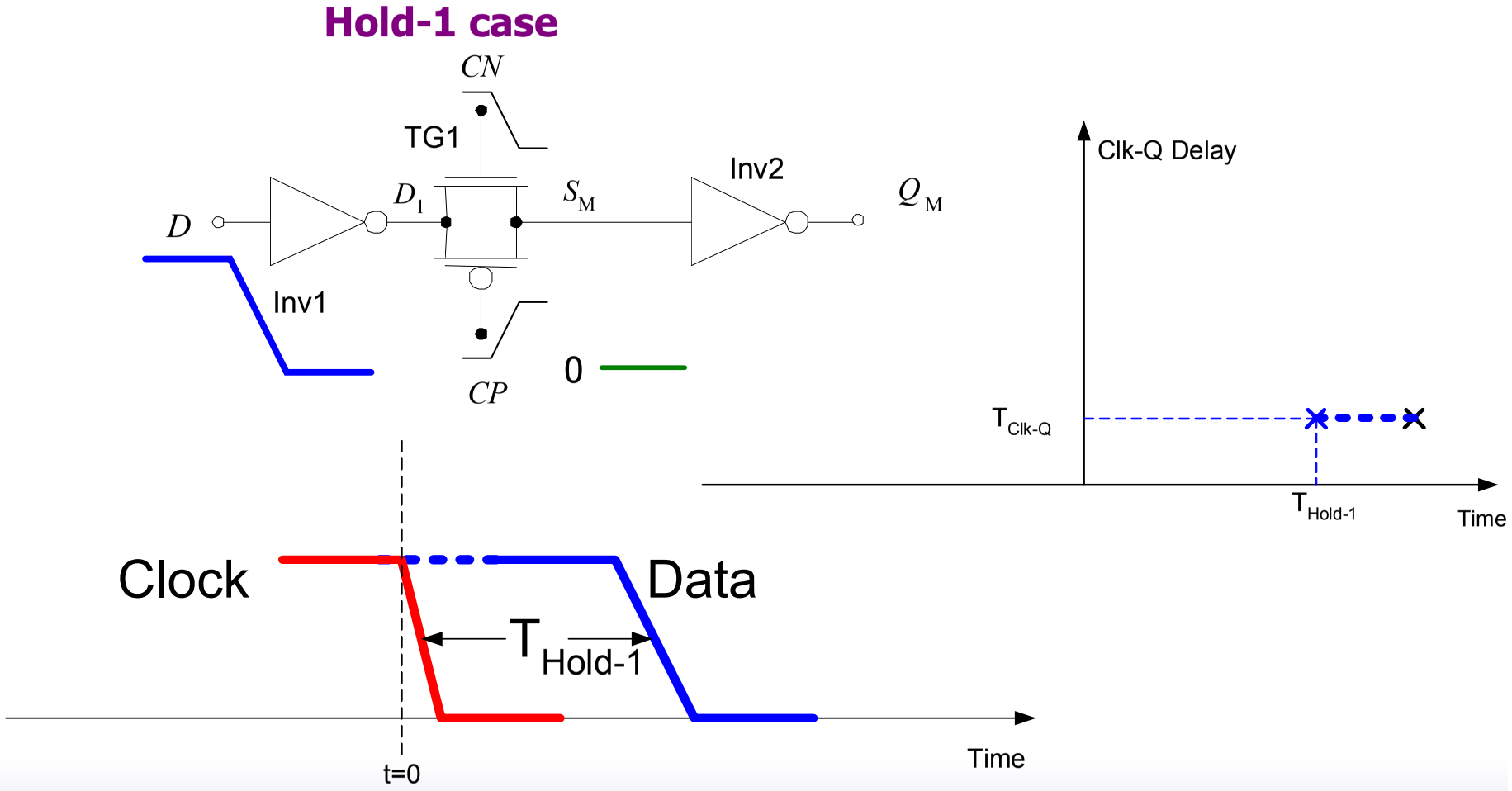

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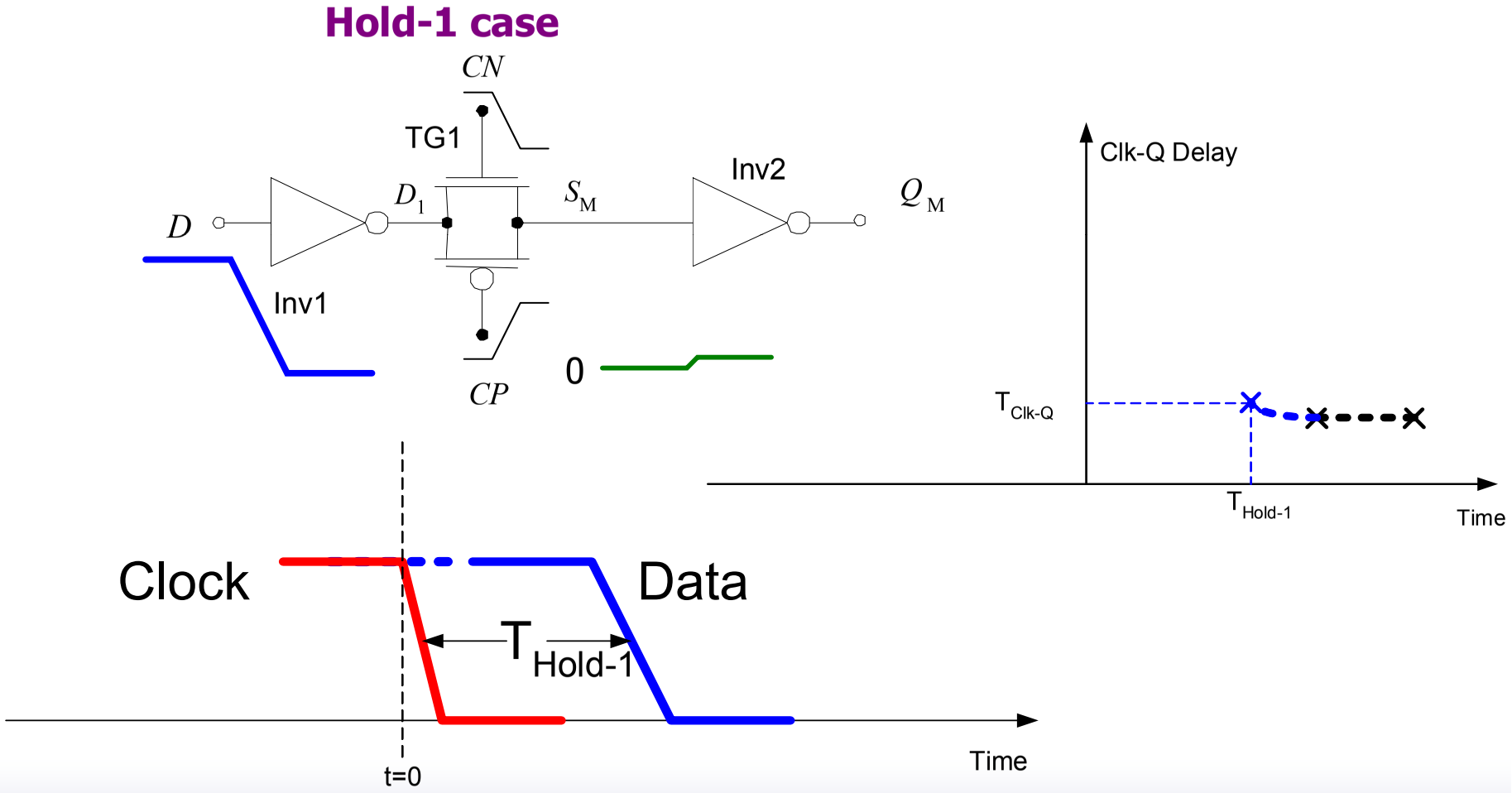

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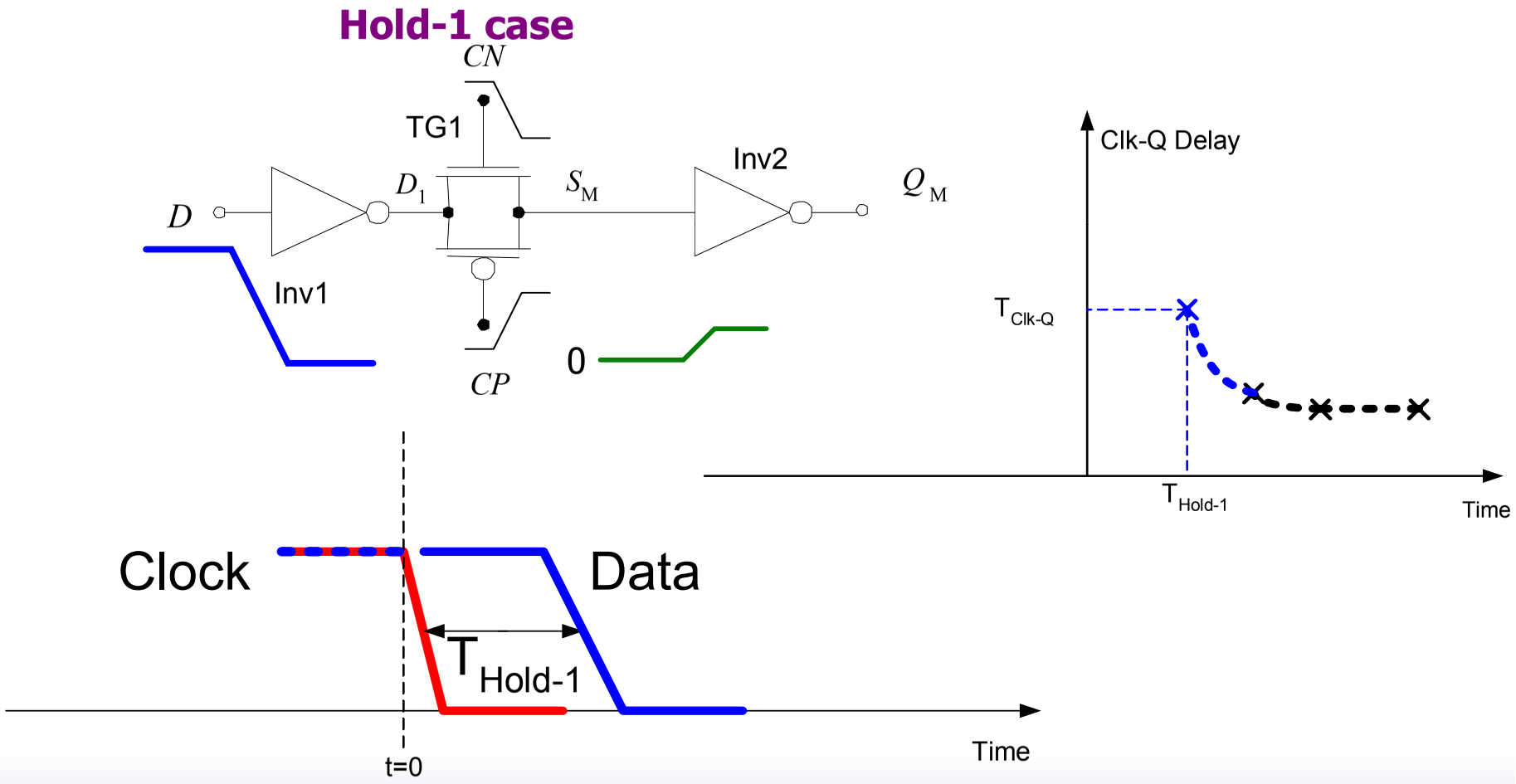

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