EECS 427
Discussion 2

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Tuesday, September 16, 2008

Administrative Stuff

- CAD2 due yesterday
  - Any questions?
- Homework 3 due two weeks from Thursday (Oct. 2)
- CAD3 due Friday, Sept. 26
  - First group assignment (rest are in groups)

Signal Naming Conventions

- Some tools can't differentiate between upper case and lower case, so net "A" and net "a" would be shorted together
- To avoid this problem do NOT name your signals with any upper case characters
- It is a good idea to label some of the intermediate net manually for later simulation debug
- Normal naming convention
  - Add "_b" for inverted signal
  - Add "n" or "_n" for active low signal

Cell Naming Conventions

- Common cells such as inverter and nand2 might exist in many of your designs
- Multiple drive strengths of the same logic cell might be needed in the same design
- To avoid cell Name duplication, add your initial or functional block name in front of the logic gate, and add the power strength after the logic gate name
  - Example: ALU_nand2X4
  - Example: RF_tribuf

Normal and high resistive transistors

- High resistive transistors are only used in keeper and feedback circuit. They are only different in their functional views. Their layouts are the same as a normal devices.

Metal Routing Topology

- Poly – any direction (typically <1um in length)
- M1 – any direction
- M2 – vertical
- M3 – horizontal
- M4 – vertical

Metal Usage in Design Hierarchy

- Large designs are usually partitioned into levels of hierarchy: chip, island, partition, unit, macro, cell
- In lower levels, only a small number of layer are allocated for routing
- Metal Layer Usage
  - Chip: all 8
  - Processor (datapath+control): up to 6
  - Datapath: up to 4
  - Macro (ALU, shifter, and RF): up to 3

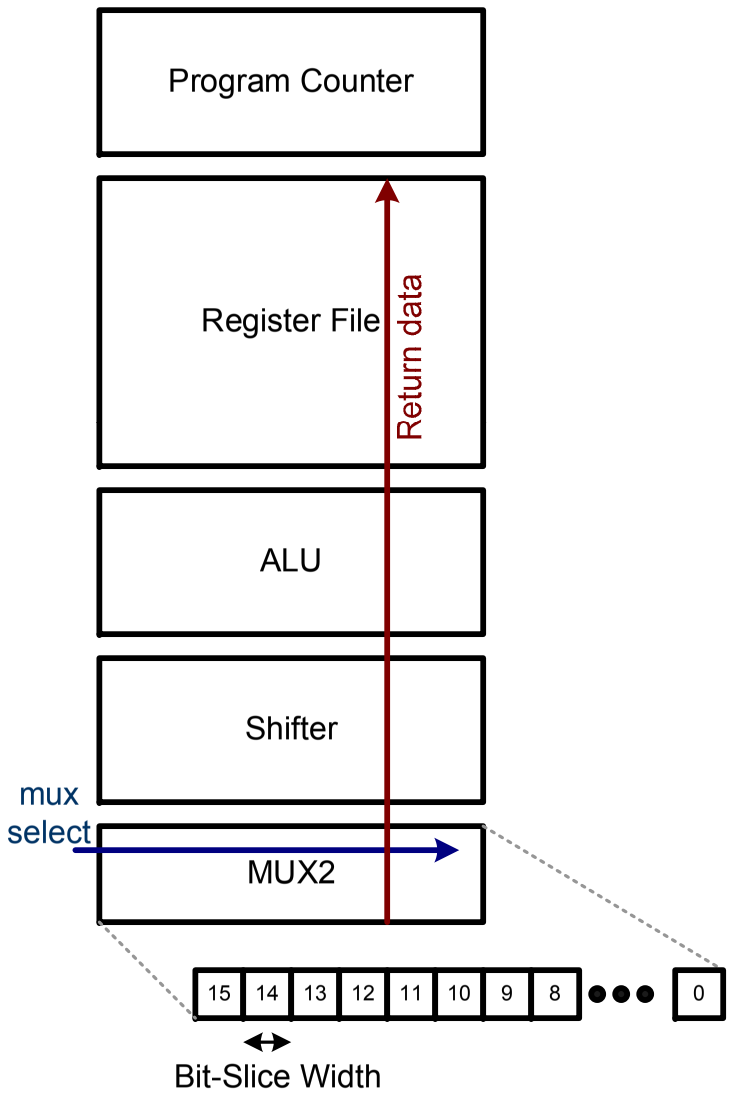
Bit Slice Width

- Bit-slice width is layout width that is allocated for one bit of computation
- It controls the aspect ratio of your final design
- It helps to establish regularity
- Width matching avoids having the data busses over the datapath turn corners
- Easier to visualize the wiring track, and estimate the wire load

Effect of the Bit-Slice Width

- A row of mux2's in the pipeline
- Large bit-slice width → long select line (blue wire)
- Small bit-slice width → long data line (red wire)

- Analyze your design to see how many wiring tracks are needed before deciding on a bit pitch



M2 Wire Usage

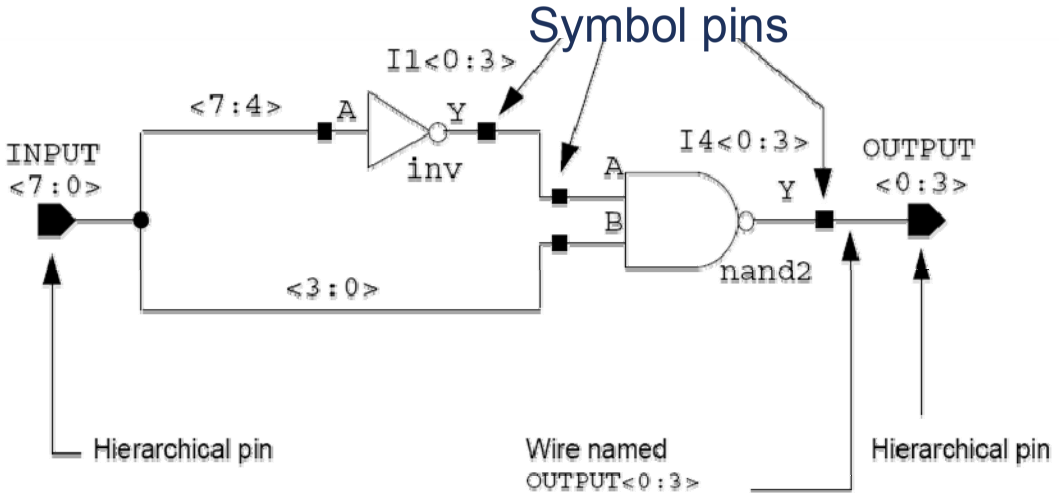
- Engineers visualize a design with fully populated wires and call the center line of those wires, “tracks.” It eliminate miscommunication between engineers.
- To make the most efficient use of your M2 wire, your bit pitch should be a multiple of 0.4um. (m2 width +m2 spacing).
- This will maximize the number of m2 routing track and reduce re-visiting your design later to allow more wire to be routed through.

Power Grid

- In robust designs, a power grid is usually included
- When you design your cell, you must make all the cells placed in the same row the same height (cell pitch matching), so that the power supply will be a continuous strip
- Wide metal are used in the power grid so that multiple vias are placed at the intersection of power grid. In our design we will have at least 4 vias at each intersection. [CAD3 requirement]
- Each bit should have a VDD and GND M2 power stripe close by [CAD3 requirement]

CAD3

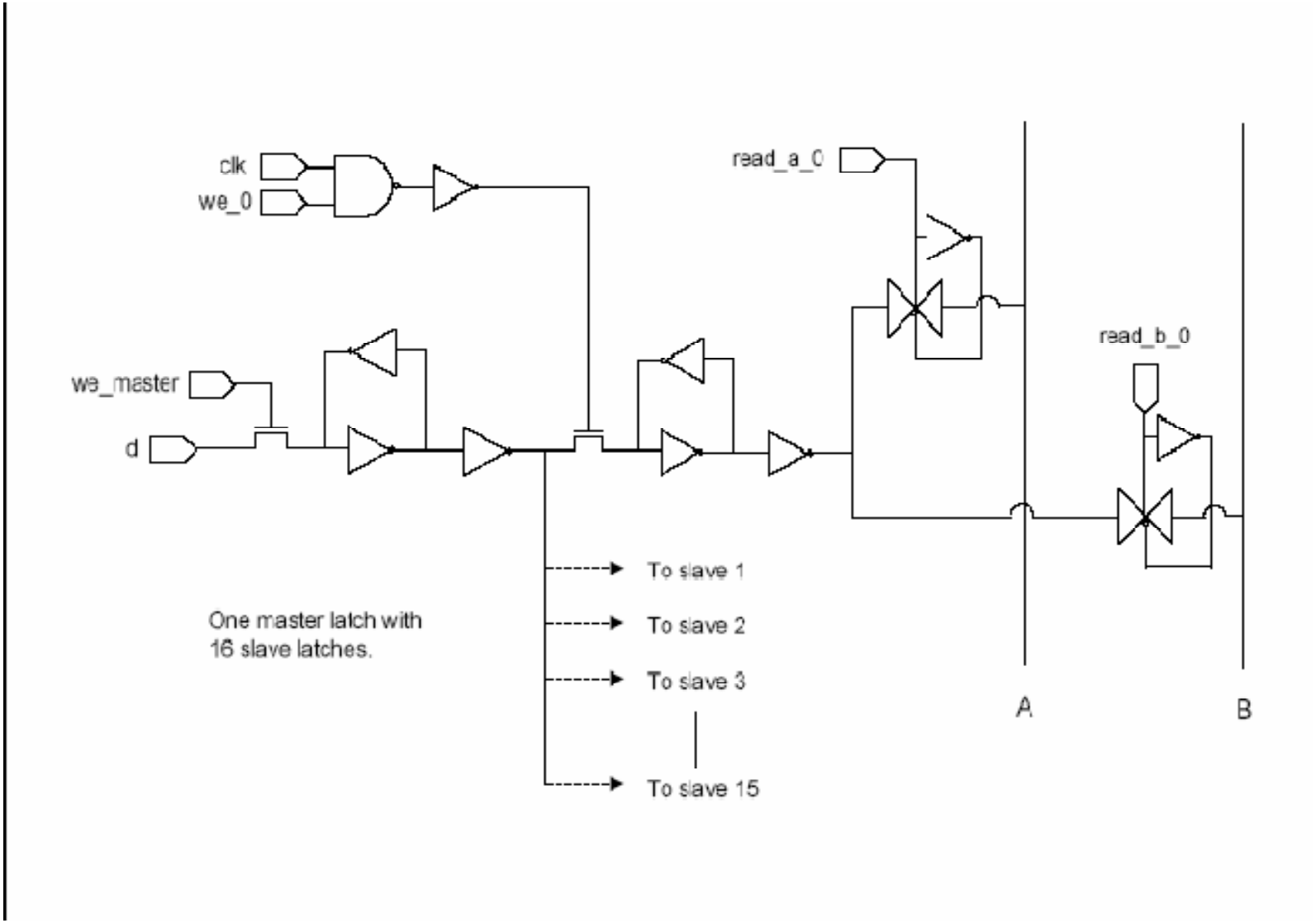
- **Take advantage of the design hierarchy!!**
- Use vector notation for both busses and instances



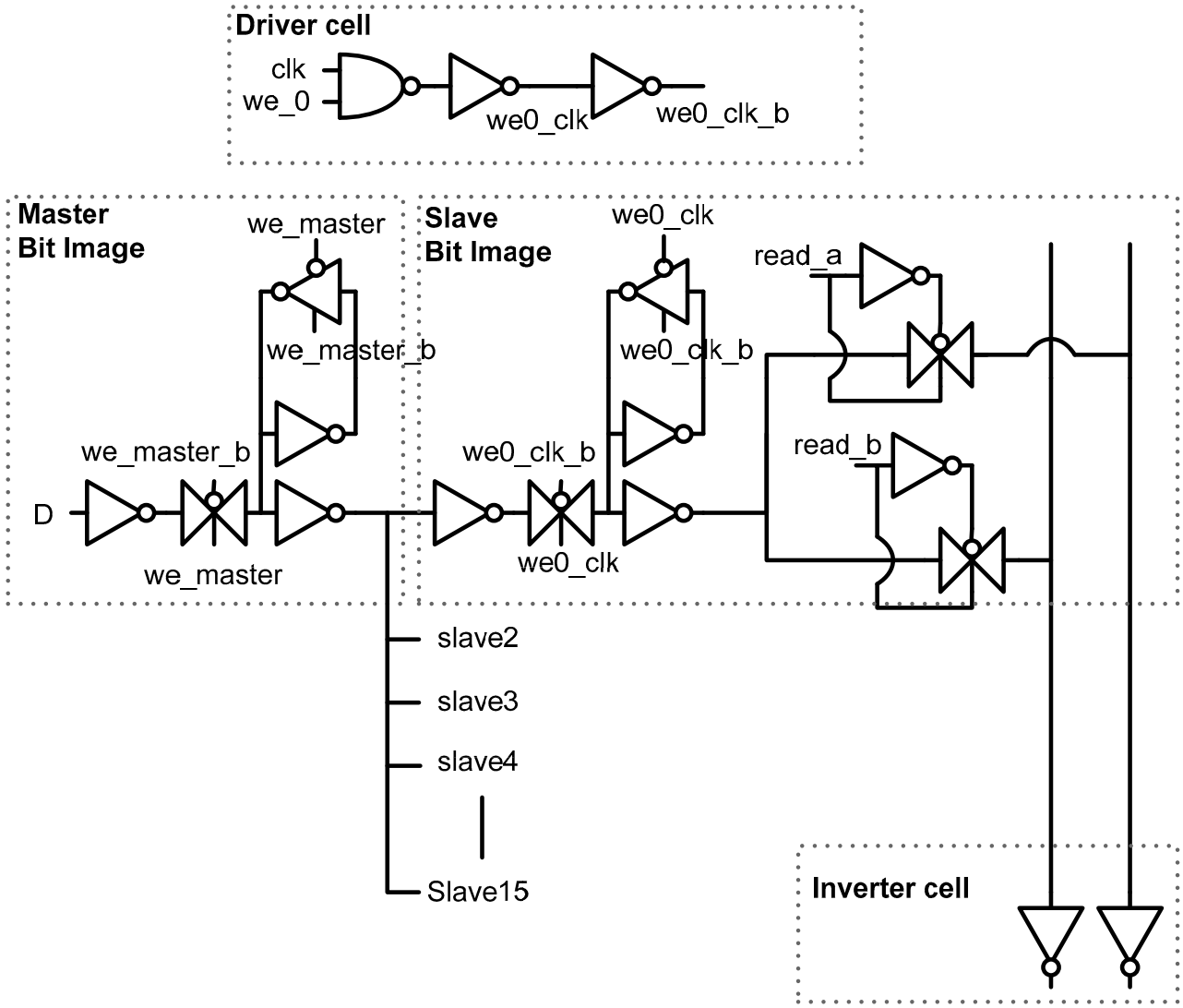
- Bus handouts for *Cadence* are included online
- The input and output signal polarity are not important.
- Reset is not required, but you should think about a way to reset your RF in the system

- ***Speed-path simulation is a very important part of CAD3***

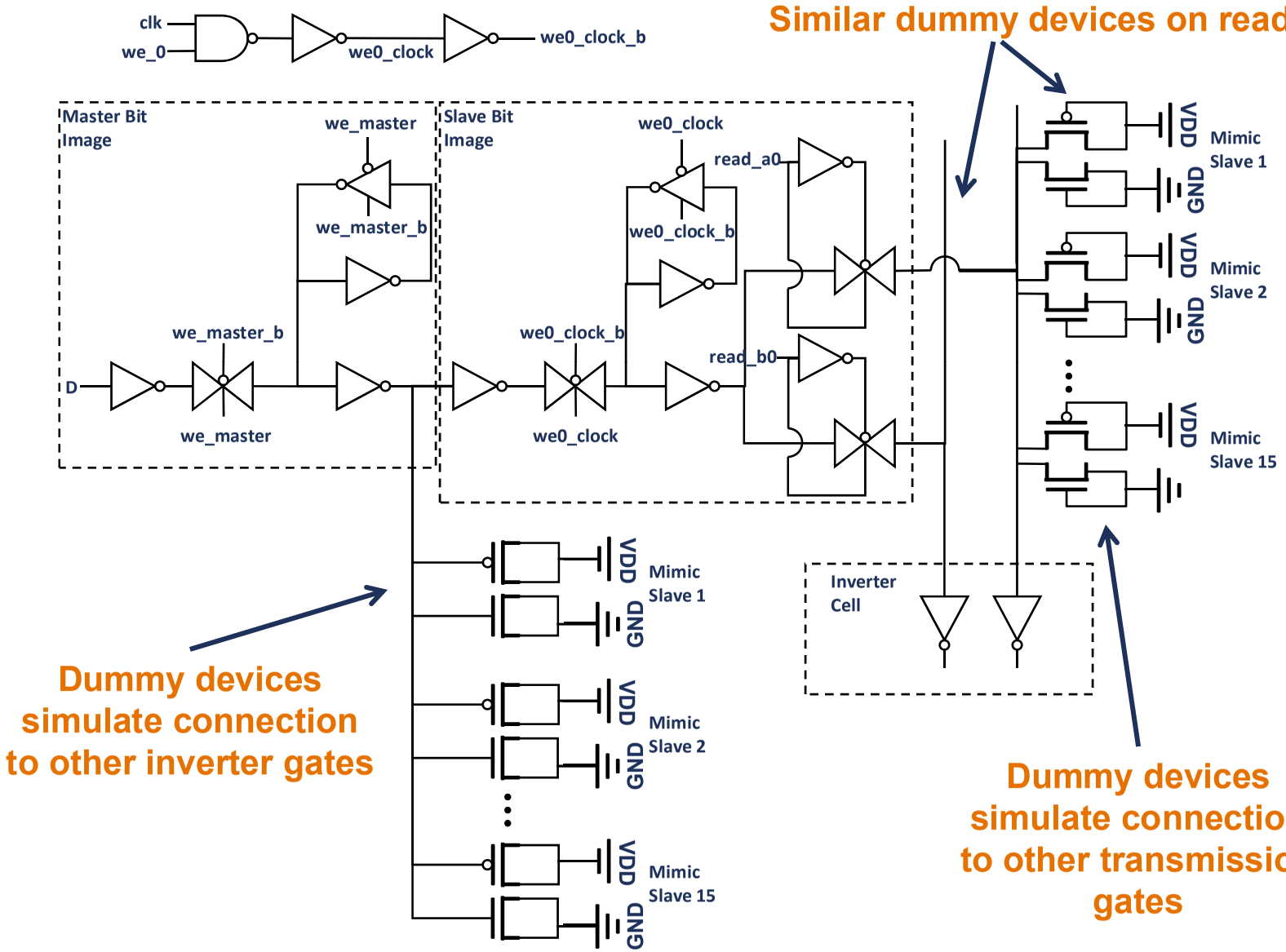
RF Bit image


clk
we_0
read_a_0
read_b_0
we_master
d
To slave 1
To slave 2
To slave 3
To slave 15
One master latch with
16 slave latches.
A
B

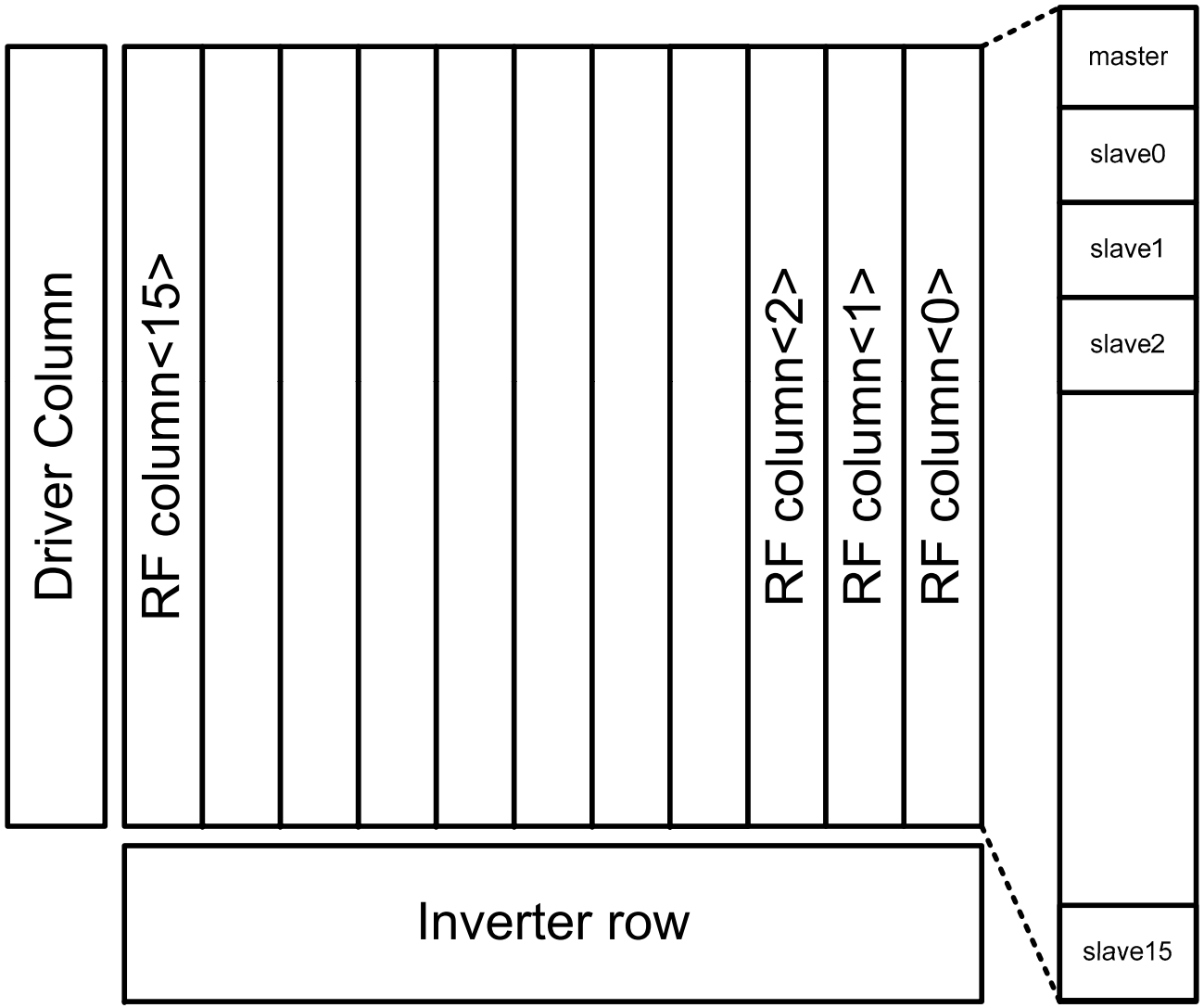
Alternative RF Bit Image



Speedpath


clk
we_0
we0_clock
we0_clock_b
Similar dummy devices on read_b
Master Bit Image
we_master
we_master_b
we_master_b
D
we_master
Slave Bit Image
we0_clock
read_a0
we0_clock_b
we0_clock_b
read_b0
we0_clock
VDD
GND
Mimic Slave 1
Mimic Slave 2
Mimic Slave 15
Inverter Cell
Dummy devices simulate connection to other inverter gates
Dummy devices simulate connection to other transmission gates

RF Hierarchy



EECS427 baseline ISA

- 16-bit RISC processor
- 2 stage pipeline: Fetch, Execute
- ~50 instructions in ISA

Baseline RISC Architecture