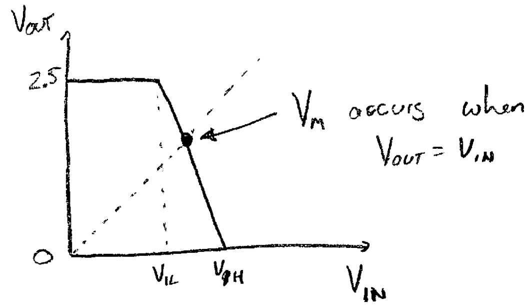
EECS 427 - F08 - HW1 SOLUTIONS

1a) $NM_L = V_{IL}$ so $V_{IL} = 1.15\text{ V}$
$NM_H = V_{DD} - V_{IH}$ $\quad V_{IH} = 2.5 - 1.1 = 1.4\text{ V}$



V_m will fall on the sloped line, so let's define it.

$$\text{slope} = \frac{\Delta y}{\Delta x} = \frac{-2.5}{1.4-1.15} = -10$$

$$V_{OUT} = -10\, V_{IN} + b$$

$$2.5 = -10 \cdot 1.15 + b \quad \Rightarrow b = 14$$

so $V_{OUT} = -10\, V_{IN} + 14$

V_M occurs when $V_{OUT} = V_{IN}$

$$V_M = -10\, V_M + 14$$

$$\underline{V_M = 1.\overline{27}\text{ V}}$$

By equating the NMOS + PMOS current, we get the following (see p185 of Rabaey)

$$\underbrace{V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r}}$$

where $r = \dfrac{k_p'\left(\frac{W_p}{L}\right) V_{DSATp}}{k_n'\left(\frac{W_n}{L}\right) V_{DSATn}}$

solve for r: $\quad r = \dfrac{\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right)}{\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2} - V_M\right)} = 1.6125$

from the defn of r, we get $\quad W_n = \frac{1}{r} \cdot \dfrac{k_p' V_{DSATp}}{k_n' V_{DSATn}} \cdot W_p = 0.77\text{ um}$

To solve for t_{FO4}, use $t_{FO4} = \frac{1}{2}(t_{pLH} + t_{pHL}) = \frac{1}{2} \cdot 0.69 \cdot C_L (R_{eqp} + R_{eqn})$

$$R_{eqn} \approx \frac{13\text{ k}\Omega}{W_n/L_{eff}} = \frac{13\text{ k}\Omega}{.77/.2} = 3.377\text{ k}\Omega \qquad R_{eqp} \simeq \frac{31\text{ k}\Omega}{W_p/L_{eff}} = \frac{31\text{ k}\Omega}{3/.2} = 2.067\text{ k}\Omega$$

$$C_L = \underbrace{4C_{gc,p} + 4C_{gc,n}}_{\text{4 fanout inverters}} + \underbrace{\tfrac{1}{2}C_{gc,p} + \tfrac{1}{2}C_{gc,n}}_{\text{self-loading}} = 4.5(C_{gc,p} + C_{gc,n})$$

For transistors in cutoff, $C_{gc} = C_{ox} W L_{eff}$

$$C_{gc,n} = 6\text{ fF/um}^2 \cdot .77\text{ um} \cdot .2\text{ um} = 0.924\text{ fF}$$

$$C_{gc,p} = 6\text{ fF/um}^2 \cdot 3\text{ um} \cdot .2\text{ um} = 3.6\text{ fF}$$

$$C_L = 4.5(C_{gc,n} + C_{gc,p}) = 4.5(.924 + 3.6) = 20.358\text{ fF}$$

$$t_{FO4} = \tfrac{1}{2} \cdot .69\, C_L (R_{eqp} + R_{eqn}) = \tfrac{1}{2} \cdot .69 \cdot 20.358 \times 10^{-15} (3.377 + 2.067) \times 10^3 = \boxed{38.2\text{ ps}}$$

1b) Since $\frac{\mu_n}{\mu_p} = 2.5$ and we want equivalent rise and fall transitions for this problem, we need $\frac{W_p}{W_n} \simeq 2.5 \quad \therefore W_p = 2.5\,W_n$

- Delay through first inverter:

$$t_p = \tfrac{1}{2} \cdot .69\, C_L (R_{eqn} + R_{eqp}) = .345 \left(\frac{13000}{1/.2} + \frac{31000}{2.5/.2} \right) C_L = 1752.6\, C_L$$

$$C_L = \tfrac{1}{2}\left[C_{gcp,inv1} + C_{gcn,inv1}\right] + C_{L,1} + C_{gcp,inv2} + C_{gcn,inv2}$$

$$= \tfrac{1}{2}\left[C_{ox} W_{p,inv1} L_{eff} + C_{ox} W_{n,inv1} L_{eff}\right] + C_{L,1} + C_{ox} W_{p,inv2} L_{eff} + C_{ox} W_{n,inv2} L_{eff}$$

$$= \tfrac{1}{2} \cdot 6\,\text{fF}/\mu m^2 \cdot .2\,\mu m\,(2.5\,\mu m + 1\,\mu m) + 10\,\text{fF} + 6\,\text{fF}/\mu m^2 \cdot .2\,\mu m\,(W_{p,inv2} + W_{n,inv2})$$

$$= 12.1 + 1.2\,(W_{p,inv2} + W_{n,inv2}) \quad \text{with } W_{p,inv2} = 2.5\,W_{n,inv2} \quad C_L = 12.1 + 4.2\,W_{n,inv2}$$

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so $t_{p,inv1} = 1752.6\,(12.1 + 4.2\,W_{n,inv2}) \times 10^{-15}$

- Delay through second inverter:

$$t_{p,inv2} = \tfrac{1}{2} \cdot .69 \cdot C_L (R_{eqn} + R_{eqp}) = .345 \left(\frac{13000}{W_n/.2} + \frac{31000}{2.5W_n/.2} \right) C_L = \frac{1752.6}{W_n} \cdot C_L$$

$$C_L = 40\,\text{fF} + \tfrac{1}{2}\left[6\,\text{fF}/\mu m^2 \cdot .2\,\mu m \cdot 3.5\,W_n\right] = 40 + 2.1\,W_n$$

$$t_{p,inv2} = \frac{1752.6}{W_n}(40 + 2.1\,W_n) \times 10^{-15}$$

$$t_p = t_{p,inv1} + t_{p,inv2}$$

This is minimized when $\underline{W_n \simeq 3.09\,\mu m}$ $\quad \underline{W_p = 2.5W_n = 7.73\,\mu m}$

2) a) In the worst case, Flop1 → Flop2 will see negative skew.

Flop1→Flop2: $T = T_{CLK\text{-}Q} + T_{LOGIC1} + T_{SETUP} - (-\delta) = 150\,ps + 1500\,ps + 75\,ps + 75\,ps = 1800$

Flop2→Flop3: $T = 150 + 80 + 75 + 75 = 380\,ps$

Flop1 → Flop2 is the worse path, and sets the max frequency.

$$f = \frac{1}{T} = \frac{1}{1800\,ps} = \boxed{556\text{ MHz}}$$

b) Since the flop2 → flop3 path has lower delay, it is limiting.

$$T_{hold} < T_{CLK\text{-}Q} + T_{LOGIC2} + \delta$$

→ In worst case, δ is positive!

$$T_{hold} < 150\,ps + 80\,ps + 75\,ps$$

$$\boxed{T_{hold,max} = 305\,ps}$$

3) Ignoring skew/jitter,

$$T = T_{CLK-Q} + T_{LOGIC} + T_{SETUP} = 200 + \frac{1600}{t} + 1000 + t$$

T_{min} occurs when $t = 40\text{ps}$

$$T_{min} = 200 + \frac{1600}{40} + 1000 + 40 = 1280\text{ ps}$$

$$f_{max} = \frac{1}{T_{min}} = \boxed{781.25\text{ MHz}}$$

4) a) $X = (A+B+C)(D+E)F + GH$ Rewrite in a more "CMOS-friendly" form

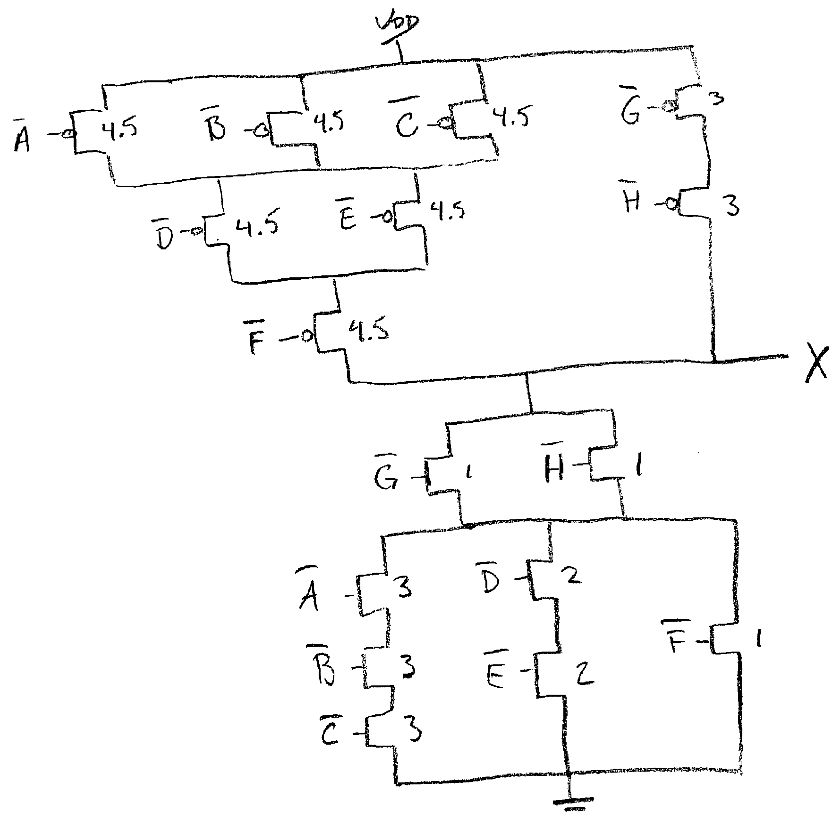
$$= \overline{\overline{(A+B+C)(D+E)F + GH}}$$

$$= \overline{\overline{(A+B+C)(D+E)F} \cdot \overline{GH}}$$

$$= \overline{[\overline{A+B+C} + \overline{D+E} + \overline{F}][\overline{G}+\overline{H}]}$$

$$= \overline{(\overline{A}\cdot\overline{B}\cdot\overline{C} + \overline{D}\cdot\overline{E} + \overline{F})(\overline{G}+\overline{H})}$$

Size all paths to be $W_p/W_n = \frac{1.5}{.5}$



Numbers are transistor widths, in microns.

b)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

XNOR $Y = A \overline{\oplus} B$

5) Lets say that all power is consumed when a node goes high (actually, ½ is consumed when it goes high, ½ when it goes low, but you will get the same answer both ways)

so $P_{dyn} = C_L V_{DD}^2 f_{0\to1}$ where $f_{0\to1}$ is the frequency of $0\to1$ transitions

$[f_{0\to1} = f\,\alpha_{0\to1}]$

Let's first find the percentage of cycles when node n_3 goes high. This will happen if previously $\{n_0, n_1\} = \{0,0\}$ and one or both inputs go high.

Probability $(\{n_0, n_1\} = \{0,0\}) = 0.25$

P (n_0 stays 0, n_1 goes $0\to1$) $= 0.9 \times .1 = .09$

P (n_0 goes $0\to1$, n_1 stays 0) $= .1 \times .9 = .09$

P (n_0 goes $0\to1$, n_1 goes $0\to1$) $= .1 \times .1 = .01$

So probability $(\{n_0, n_1\} = \{0,0\})$ <u>AND</u> the output n_3 goes high is

$0.25(.09 + .09 + .01) = \underline{0.0475}$

Now, let's do the same for n_4. n_4 can go high if

a) inputs are (0,0) and they both go high $(0\to1, 0\to1)$

b) inputs are (0,1) and n_3 goes high $(0\to1, 1\to1)$

c) inputs are (1,0) and n_2 goes high $(1\to1, 0\to1)$

a) $P(n_3 = 0, n_2 = 0) = 1/8$ $\quad P(0\to1, 0\to1) = .0475 \times .1 = .00475$

so probability of (a) is $1/8 \cdot .00475 = .000594$

b) $P(n_3 = 0, n_2 = 1) = 1/8$ $\quad P(0\to1, 1\to1) = .0475 \times .9 = .04275$

Probability of (b) is $1/8 \cdot .04275 = .00534$

c) $P(n_3 = 1, n_2 = 0) = 3/8$

but what's the probability that n_3 stays a 1?

$P(n_3$ is a 1 and stays a 1$) = 1 - P(n_3$ is a 1 and transitions$)$

P(n_3 is a 1 and transitions to $\emptyset$):

$P(n_0=0, n_1=1) = 1/4$ $\quad$ $P(0\to0, 1\to0) = .9\times.1 = .09$

$P(n_0=1, n_1=0) = 1/4$ $\quad$ $P(1\to0, 0\to0) = .1\times.9 = .09$

$P(n_0=1, n_1=1) = 1/4$ $\quad$ $P(1\to0, 1\to0) = .1\times.1 = .01$

since $P(n_0=0, n_1=1) = P(n_0=1, n_1=0) = P(n_0=1, n_1=1)$

given that $n_3 = 1$, the probability n_3 transitions is $\frac{.09+.09+.01}{3} = .06\bar{3}$

using this to find out (c) above,

c) $P(n_3=1, n_2=0) = 3/8$ $\quad$ $P(1\to1, 0\to1) = .06\bar{3}\times.1 = .006\bar{3}$

So the probability n_4 goes $0\to1$ is (from (a), (b), and (c))

$.00594 + .00534 + .00633 = 0.0176$

Now, assuming that power is only used in this circuit when n_3 and n_4 switch,

$$P_{dyn} = C_L V_{DD}^2 f \alpha_{0\to1} = 10fF\times(2.5V)^2\cdot 1GHz\cdot(.0475+.0176)$$
$$= \boxed{4.1\ \mu W}$$

If you want to include n_0, n_1, and n_2, you will get

$$P_{dyn} = 10fF(2.5V)^2\cdot 1GHz\cdot(.0475+.0176+.05+.05+.05)$$

remember we're only looked at $0\to1$ transitions

$$= \boxed{13.4\ \mu W}$$