EECS 427, Winter 2007
HW1 (review)

Technology Parameters

- Minimum drawn channel length = 0.25μm; Effective channel length for L_{drawn} of 0.25 μm = 0.2 μm; V_{dd} = 2.5V.
- k_n' = 115mA/V^2; k_p' = -30mA/V^2
- V_{DsatN} = 0.63V, V_{DsatP} = -1V
- V_{TN0} = 0.43V; V_{TP0} = -0.4V.
- γ_n =0.4; γ_p = - 0.4;
- C_{ox} = 6fF/ μm^2
- Assume junction capacitance of a MOSFET , C_{jd}, C_{js} is equal to half the gate-to-channel capacitance C_{gc}. That is, $C_{gc} = 2C_{jd} = 2C_{js}$.

1.0 – Combinational Logic Design. Using only 2-input AND gates and 2-input OR gates, implement a 3-input majority function.

1.1 – Now implement the same function using only 2-input NAND gates.

1.2 – Given the function below, draw the corresponding CMOS gate. Also, re-write OUT using DeMorgan's theorem to more clearly represent the pull-up network.

$$OUT = \overline{E + ((D \bullet A) + (B \bullet C))}$$

2.0 – Consider the static CMOS nand gate shown in Figure 1. Ignoring junction leakage and subthreshold current, determine the voltage of node *n*.

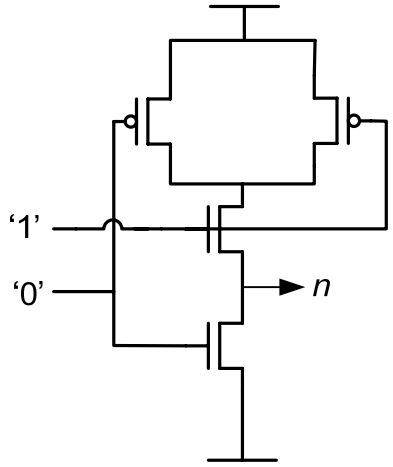

Figure 1 : CMOS NAND gate

3.0 – Given a static CMOS inverter with W_n=1 μm and W_p=1.8 μm (L_{drawn} = 0.25 μm), calculate, for a step input, t_{rise}, t_{fall}, $t_{delaylh}$ and $t_{delayhl}$ when driving (a) a 0fF load and (b) a 10fF load capacitance. Include the self loading of the inverter, that is, the junction capacitance of the transistors.

4.0 – Consider the RC network shown in Figure 2. Calculate the elmore delay from point a to b.

4.1 – What is the elmore delay from point b to a.

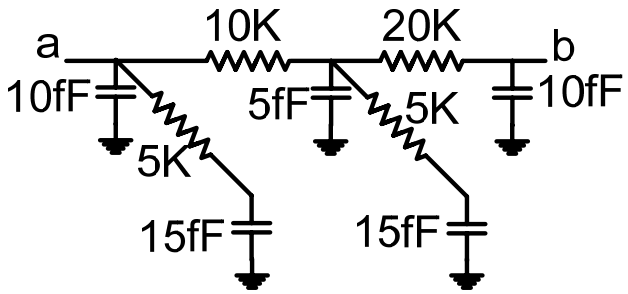

Figure 2: RC network

5.0 – Consider a source of random bits. Draw the state transition diagram of a state machine that takes the random bitstream as an input and outputs a 1 every time the last 4 bits of the bitstream were "1010".

6.0 – Consider the two situations of an inverter driving different loads shown in Figure 3. Which inverter experiences higher crowbar current upon a switching event at the input.

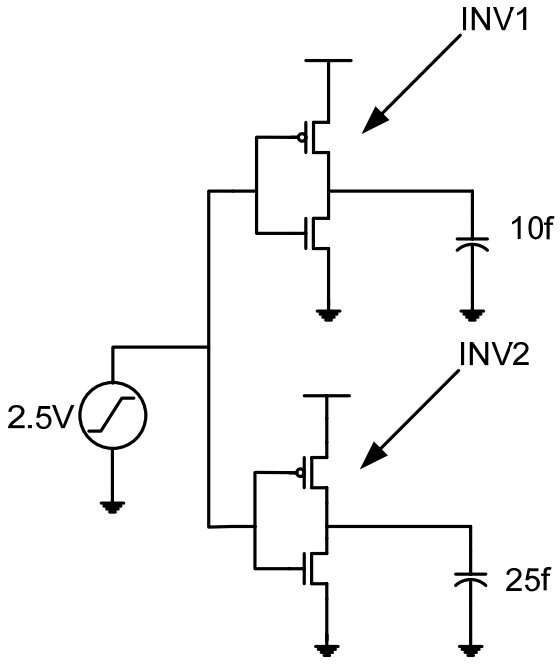

Figure 3 : Two identical inverters driving different loads.

7.0 – Consider a rectangle with length *x* and width *y*. Given that $xy = 16$, calculate the dimensions x and y so as to minimize the perimeter.

8 – Consider the sequential circuit shown in Figure 4, consisting of 3 edge-triggered flip-flops and with logic blocks A, B and C . Assume that T_{setup}=3ns, T_{hold} = 3ns, T_{CQ}=2ns.

8.0 – If $T_{comb\text{-}A}$ = 5ns, $T_{comb\text{-}B}$ = 3ns and $T_{comb\text{-}C}$ = 4ns, calculate the maximum clock frequency at which the circuit can operate correctly.

8.1 – Now assume that the clock period is 20ns. What is the maximum possible delay of the three combinational logic blocks so that the setup constraints are met? Also calculate the minimum delay constraints on each of the blocks to meet the hold-time constraints.

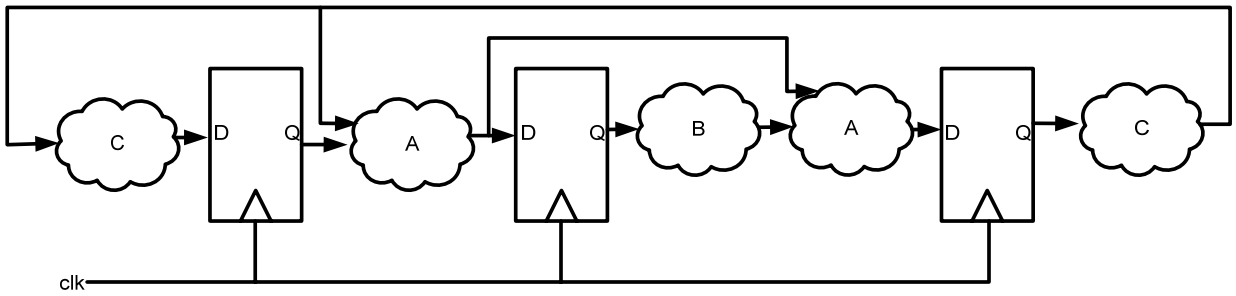

Figure 4: Sequential Circuit.