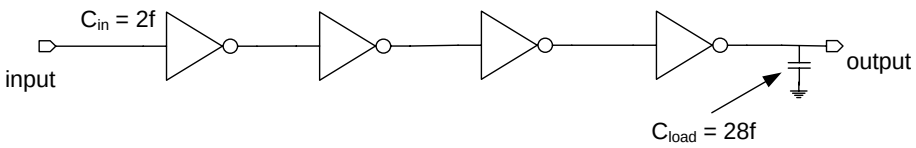
LOGICAL EFFORT SAMPLE QUESTIONS

For all questions, assume that $p_{inv}=1\tau$.



In the gate netlist shown in Figure 1, use logical effort to find the optimal gate sizes for each inverter. Can a better configuration with lower delay be achieved using only symmetric gates? How does wire capacitance between the inverters affect this result?

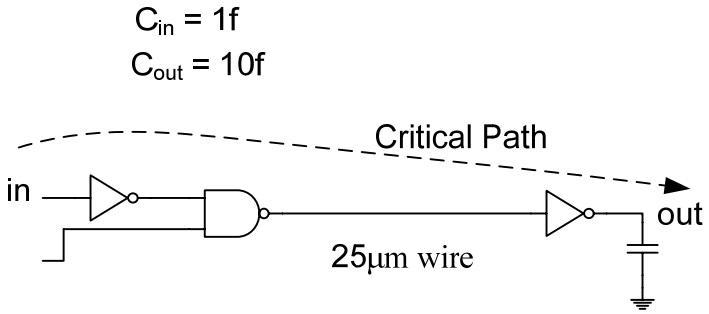
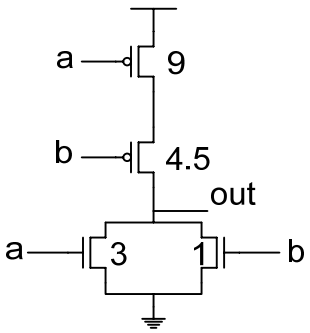


Figure 2: Gate netlist schematic.

Figure 2. shows the schematic of a critical section from in to out. The NAND gate drives a 25μm wire, which in this technology results in a 5fF load. Using logical effort, compute the optimal sizing for the gates.Also, report the total delay of the gate. Assume that the gate capacitance of a 1μm device (NFET AND PFET) is 1fF. Assume β=2 (Hint: Iterate)



For the gate in Figure 3. Assume that β=3. The critical path in the design passes from pin *b* to the output of the gate. Compute the logical effort of the gate for each input pin. Also compute the parasitic delay of the gate. Can the delay of this gate be improved further without increasing the loading of pin *a* further? Find this appropriate gate size and the resulting logical effort and parasitic delay (if different).

Assume this nand gate were then used for the netlist shown in Figure 2. Find the optimal gate sizes and the total delay using logical effort.