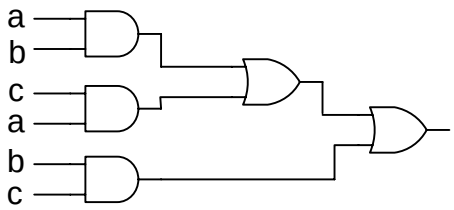
EECS 427, Winter 2007
HW1 (review) (solutions)

Technology Parameters

- Minimum drawn channel length = 0.25μm; Effective channel length for L_{drawn} of 0.25 μm = 0.2 μm; V_{dd} = 2.5V.
- $k_n' = 115mA/V^2$; $k_p' = -30mA/V^2$
- $V_{DsatN} = 0.63V$, $V_{DsatP} = -1V$
- $V_{TN0} = 0.43V$; $V_{TP0} = -0.4V$.
- $\gamma_n = 0.4$; $\gamma_p = -0.4$;
- $C_{ox} = 6fF/\mu m^2$
- Assume junction capacitance of a MOSFET , C_{jd}, C_{js} is equal to half the gate-to-channel capacitance C_{gc}. That is, $C_{gc} = 2C_{jd} = 2C_{js}$.

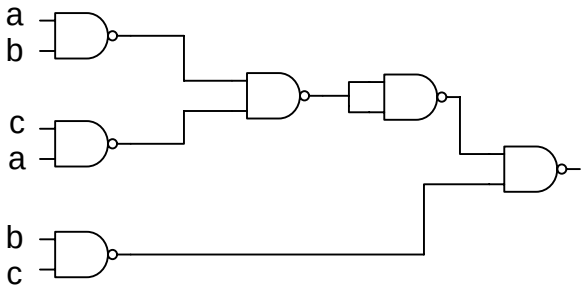
1.0 – Combinational Logic Design. Using only 2-input AND gates and 2-input OR gates, implement a 3-input majority function.

This is one implementation. There are other implementations, in fact some with fewer gates.



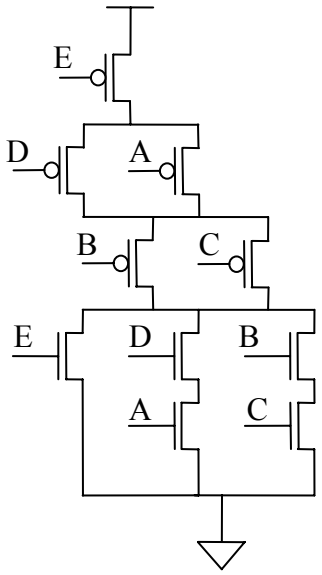
1.1 – Now implement the 3-input function using only 2-input NAND gates.

Once again, there are other implementations.



1.2 – Given the function below, draw the corresponding CMOS gate. Also, re-write OUT using DeMorgan's theorem to more clearly represent the pull-up network.

$$OUT = \overline{E + ((D \bullet A) + (B \bullet C))}$$



$$\overline{OUT} = \overline{E}(\overline{A} + \overline{B})(\overline{C} + \overline{D})$$

2.0 – Consider the static CMOS nand gate shown in Figure 1. Ignoring junction leakage and subthreshold current, determine the output voltage the node *n*.

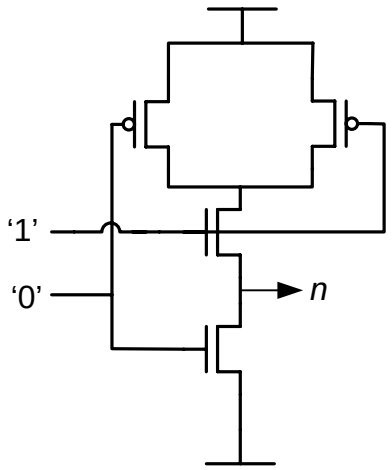


Figure 1 : CMOS NAND gate

The voltage at node n is the solution to the equation

$$V = V_{dd} - (V_{thn} + \gamma(\sqrt{V + 0.6} - \sqrt{0.6}))$$

$$V = 2.5 - (0.43 + \gamma(\sqrt{V + 0.6} - \sqrt{0.6}))$$

Solving the equation gives V=1.76V

3.0 – Given a static CMOS inverter with W_n=1 μm and W_p=1.8 μm (L_{drawn} = 0.25 μm), calculate, for a step input, $t_{rise,}$ t_{fall}, $t_{delaylh}$ and $t_{delayhl}$ when driving (a) a 0fF load and (b) a 10fF load capacitance. Include the self loading of the inverter, that is, the junction capacitance of the transistors.

(a) Before solving for , $t_{rise,}$ t_{fall}, t_{dr} and $t_{df,}$ we evaluate the load seen by the inverter when no output load is applied.

C_{gd0n} = 0.05*0.5*1*6f = 0.15f
C_{gcn} = 0.2 * 1 * 6f = 1.2f
C_{gcp} = 0.2*1.8*6 = 2.16f
C_{gd0p}=0.05*0.5*1.8*6=0.27f
C_{jn} = C_{gcn} * 0.5 = 0.6
C_{jp} = C_{gcp} = 1.08
Total load = C_{jp} + C_{jn} + C_{gd0n} + C_{gd0p} = 2.1f

Now, we compute the current in the PFET device which operates in saturation during the pull-up.

$$I_{DP} = 30 \times \frac{1.8}{0.2}\left(V_{gs}^{'} V_{dsat} - \frac{1}{2}V_{dsat}^{2}\right)$$

$$I_{DP} = 30 \times \frac{1.8}{0.2}\left((2.5 - 0.4)1 - \frac{1}{2}\right) = 432\mu A$$

The rise delay t_{drise}, is then computed as follows

$$t_{dr} = \frac{CV}{2I} = \frac{2.1 \times 2.5}{2 \times 432\mu A} = 6ps$$

The rise time t_{rise} can be computed as follows

$$t_r = \int_{0.25}^{2.25} \frac{CdV}{I} = \int_{0.25}^{1.5} \frac{CdV}{I} + \int_{1.5}^{2.25} \frac{CdV}{I(V)}$$

Substituting $x = 2.5 - V$

$$t_r = \int_{0.25}^{1} \frac{Cdx}{432\mu A \times x} + \int_{1}^{2.25} \frac{Cdx}{432\mu A}$$

$$t_r = \frac{C}{432\mu A}\left[\ln x\right]_{0.25}^{1} + \frac{C}{432\mu A}\left[x\right]_{1}^{2.25}$$

$$t_r = 6.73ps + 6.08ps$$

$$t_r = 12.81ps$$

Similarly, we compute the current in the NFET device which operates in saturation in during the pull-down

$$I_{DN} = 115 \times \frac{1}{0.2}\left(V_{gs}^{'} V_{dsat} - \frac{1}{2}V_{dsat}^{2}\right)$$

$$I_{DN} = 115 \times \frac{1}{0.2}\left((2.5 - 0.43)0.63 - \frac{1}{2}0.63^{2}\right) = 635\mu A$$

The fall delay t_{dfall}, is then computed as follows

$$t_{df} = \frac{CV}{2I} = \frac{2.1 \times 2.5}{2 \times 635\mu A} = 4.1ps$$

The fall time t_{fall} can be computed as follows

$$t_f = \int_{0.25}^{2.25} \frac{CdV}{I} = \int_{0.25}^{0.63} \frac{CdV}{I(V)} + \int_{0.63}^{2.25} \frac{CdV}{I}$$

$$t_f = \int_{0.25}^{0.63} \frac{CdV}{635\mu A \times V} + \int_{0.63}^{2.25} \frac{CdV}{635\mu A}$$

$$t_f = \frac{C}{635\mu A}\left[\ln V\right]_{0.25}^{0.63} + \frac{C}{635\mu A}\left[V\right]_{0.63}^{2.25}$$

$$t_f = 3.05ps + 5.34ps$$

$$t_f = 8.39ps$$

(b) To compute the delays for the case with a 10fF load attached, simply observe that delay is linear in C and scale the results in (a) by 12.1/2.1=5.76
Therefore
T_{rise} = 12.81 * 5.76 = 73.78ps
T_{fall} = 8.39 * 5.76 = 48.32ps
T_{drise} = 6 * 5.76 = 34.56ps
T_{dfall} = 4.1 * 5.76 = 23.616ps

4.0 – Consider the RC network shown in Figure 2. Calculate the elmore delay from point a to b.

Elmore delay from a to b, τ_{ab} = 10k*30f + 20k*10f = 50ps

4.1 – What is the elmore delay from point b to a.

Elmore delay from b to a, τ_{ba} = 20k*45f + 10k*25f = 115ps

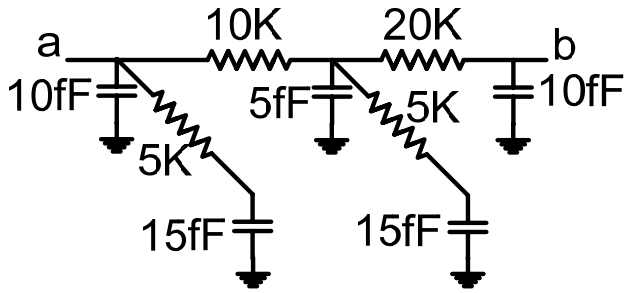
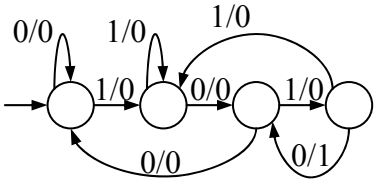


Figure 2: RC network

5.0 – Consider a source of random bits. Draw the state transition diagram of a state machine that takes the random bitstream as an input and outputs a 1 every time the last 4 bits of the bitstream were "1010".

The state transition diagram implemented as a mealy machine looks like:



6.0 – Consider the two situations of an inverter driving different loads shown in Figure 3. Which inverter experiences higher crowbar current upon a switching event at the input.

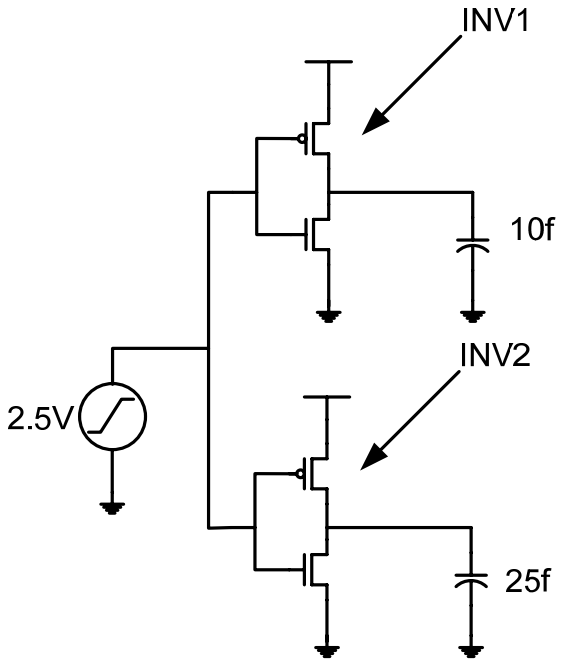


Figure 3 : Two identical inverters driving different loads

Inverter INV2 experiences lower crowbar current than INVX1. This is because for the same input signal, V_{ds} in the non-conducting device is higher for the inverter driving a lower load. For example if the input transitions from 0 to 1, the output of INV1 will fall towards 0 faster then that of INV2 while the input signal is transitioning. The PMOS device, which conducts the short-circuit current experiences higher current in INV1 since $V_{ds} = V_{dd} - V_{out}$ is higher in INV1 than in INV2

7.0 – Consider a rectangle with length *x* and width *y*. Given that $xy = 16$, calculate the dimensions x and y so as to minimize the perimeter.

Solved in class. Substitution indicates that the optimal value is when x=y=4.

8.0 – Consider the sequential circuit shown in Figure 4, consisting of 3 edge-triggered flip-flops and with logic blocks A, B and C . Assume that T_{setup}=3ns, T_{hold} = 3ns, T_{CQ}=2ns.
a) If T_{combA} = 5ns, T_{comb-B} = 3ln and T_{comb-C} = 4ns, calculate the maximum clock frequency at which the circuit can operate correctly.

The longest path, by inspection is A + A + C = 14ns. The minimum clock period is therefore 14+T_{setup} + T_{CQ} = 19ns for a maximum clock frequency of about 52Mhz

b) Now assume that the clock period is 20ns. What is the maximum possible delay of the three combinational logic blocks so that the setup constraints are met? Also calculate the minimum delay constraints on each of the blocks to meet the hold-time constraints.

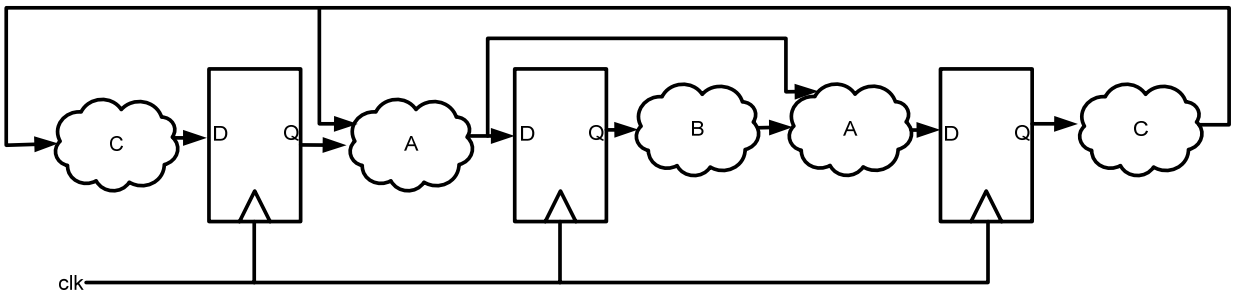


Figure 4: Sequential Circuit.

Considering the stage with 2 C blocks,: 2C + T_{setup} + T_{CQ} < 20
Therefore, C<7.5
Now the stage with C+2A: C+2A+ T_{setup} + T_{CQ} < 20
Therefore, A<7.5 - C/2 (3.75 if C is at maximum of 7.5)
Finally, B+A+ T_{setup} + T_{CQ} < 20
So, B<15-A (11.25 if A is at 3.75)

For hold time there is a single A path so A+ T_{CQ}>3 : A>1
B is only ever in line with A so A+B+T_{CQ}>3 : A+B>1 : no constraint on B (A>1)
C sees a path with A which puts no constraint on C and a path with 2 Cs so 2C>1 : C>0.5