EECS 427
VLSI Design I

TuTh 9:00-10:30am
Disc: Tu 5:30-6:30
Prof. Joel VanLaven

http://www.eecs.umich.edu/courses/eecs427

Outline

- What you can expect to learn in this class
- Logistics – teaching staff intro, go over syllabus
- CMOS processing sequence

What you will learn in 427

- 312 – Transistors design and behavior
- 270 – Logic design – combining transistors
- 370 – Architecture – high level organization

- *427* – VLSI: realization of circuits in silicon:
  - The entire process of very large-scale integration
  - Generation of custom layout
  - Sub-system design such as adders, register files..
  - Synthesis + automated place/route design flow
  - Advanced circuit design topics: pulsed latches, memory decoder and sense amplifiers, power, etc.

  Project - Teamwork

Teaching Staff

- Primary instructor:
  - Joel VanLaven
    - office hours: Wedneday 1:00 – 4:00pm, Thursday 4:00 – 6:00pm, Friday 1:00-4:00pm.
    - Background in CSE Theory and Architecture (GSI for 470 for 3 terms)
    - Job as CAD tool support for the department and College
- GSI:
  - Visvesh Sathe
    - office hours: Monday 2:00 – 6:00pm, Tuesday 11:00 – 1:00pm, Thursday 2:00-4:00pm.
    - Background in VLSI and EE (about to get PhD in VLSI)

Course setup

- Tues and Thur lectures in 1311 EECS
- Tuesday discussion section (1003 EECS)
  - Some discussions: will be like lectures, more focussed on project details. Some review of lecture topics, CAD assignments, and answer project related questions
- Homeworks
  - Only 1 ‘typical’ HW, others handle planning issues of project (groups, initial proposal, etc.)
- CAD assignments
  - Roughly weekly, several 2+week assignments
  - Each assignment represents a component of your final microprocessor design
  - First 2 (and one in middle) are individual, rest are in groups
- Quizzes: 3 - roughly every 4 weeks, non-cumulative.

Project

- Main component of class, 70+% of your grade
- Design a 16-bit RISC (reduced instruction set computing) processor
  - Groups of 4 (you choose)
    - Good to have a mix of EE and CE/CSE
    - Baseline architecture (instruction set) given to you; you choose an application and add special instructions / peripherals
  - Time requirements: 30-40 hrs/week avg. 427 is 24/7
  - Peer contribution forms; must pull your weight
- Learn full-custom design (datapath) and automation tools (logic synthesis + custom router + place/route)
- You can send this design off to be fabricated and then test it later as a directed study or possibly in EECS 579 (encouraged!)
- Warning: New tools and CAD flow this year!

Logistics

- Course Textbook:
  Digital Integrated Circuits: A Design Perspective, 2nd edition by Rabaey, Chandrakasan, and Nikolic

- Lecture notes will be posted online shortly after class sessions and I will bring copies to class for note taking
- Book will be supplemented with several handouts from other sources throughout the semester
- Other books on reserve at Media Union (Weste, Chandrakasan)
  - Weste/Harris in particular is recommended if you want to pursue a career/graduate studies in digital circuits

Grade Breakdown

- Your project, in the form of CAD assignments and final report/presentation, is the dominant part of your grade

Homework	10%
CAD assignments	35%
Quizzes	24% (8% each)
Final project/report, indiv. contrib.	31%

CAD late policy: within 24 hours = 25% penalty, 24-48 hours = 50% penalty, see course info handout

Project Schedule

- *Tutorial* 1 (CAD)
- CAD1 (inverter/nand/mux) individual
- CAD2 (D flip-flop) individual
- CAD3 (register file)
- *Tutorial* 2 (router)
- CAD4 (ALU)
- CAD5 (shifter)
- *Tutorial* 3 (verilog):
- CAD6 (PC) individual
- CAD7 (datapath)
- CAD8 (controller)
- CAD9 (completion)

Lecture Schedule Overview

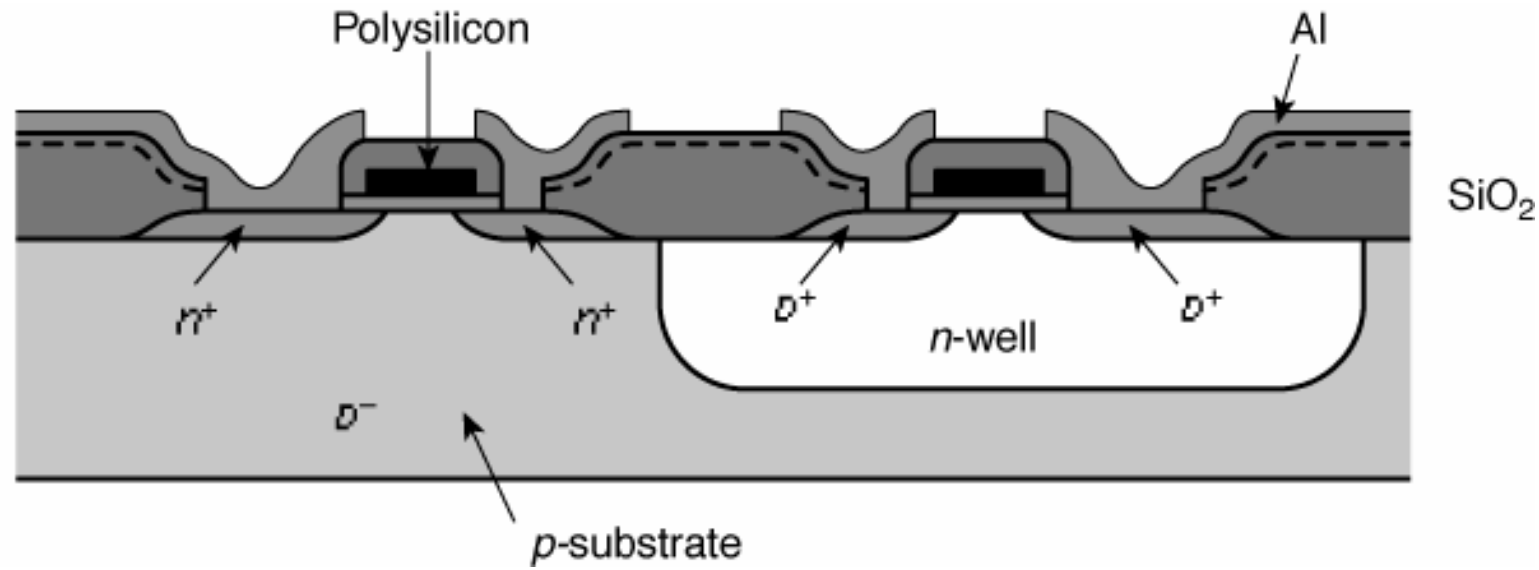
- First third is review and basics you need to get started
- Second third is mostly designs of things related to the project
- Last third is mostly advanced topics that are interesting but probably won't make it into your project.

- Schedule is tentative and subject to change
- Detailed summary should show on page when you mouse over item

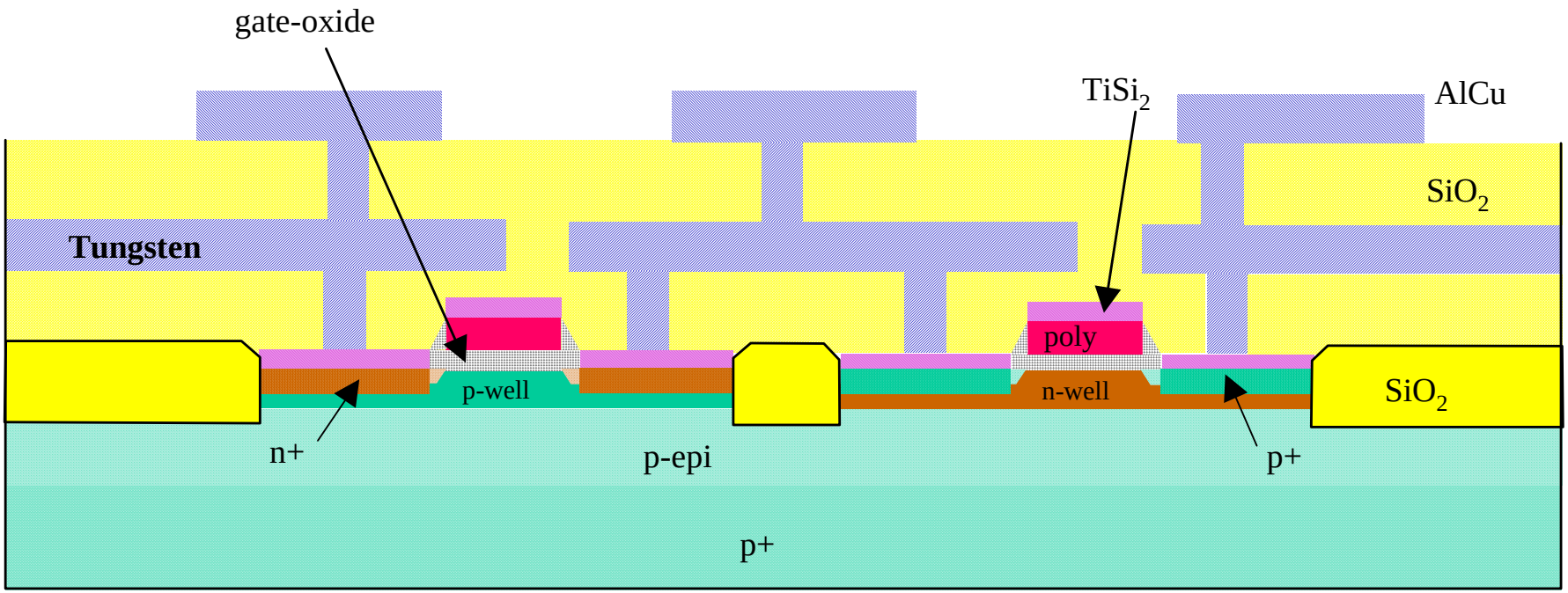
- http://www.eecs.umich.edu/courses/eecs427/w07/schedule.html

5 Minute break!

CMOS Process

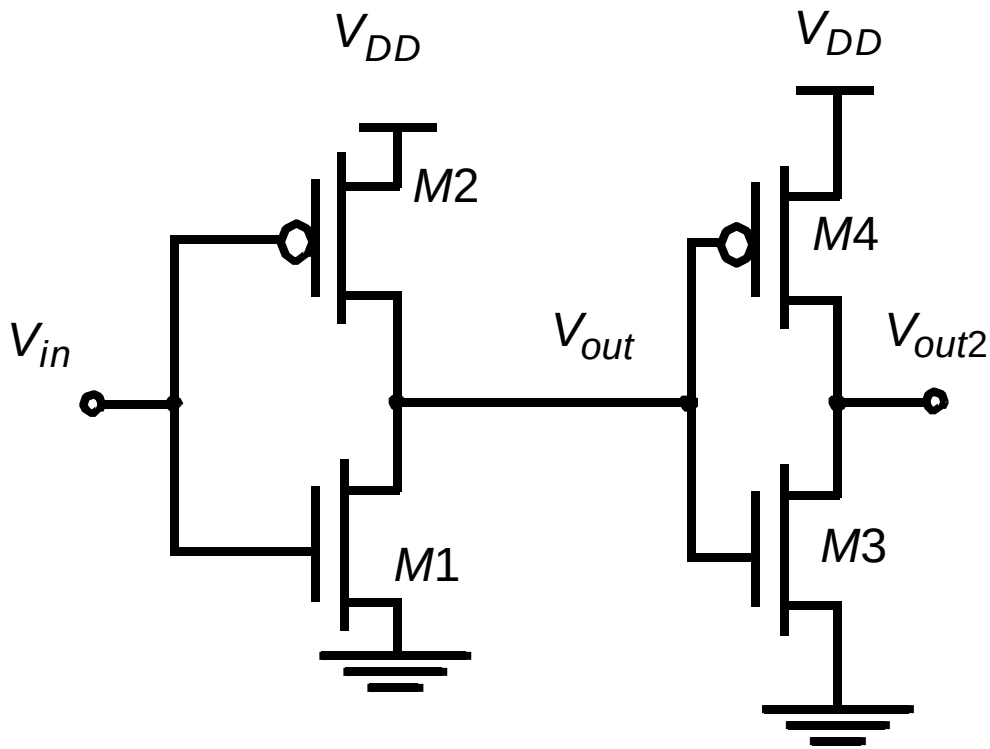


A Modern CMOS Process

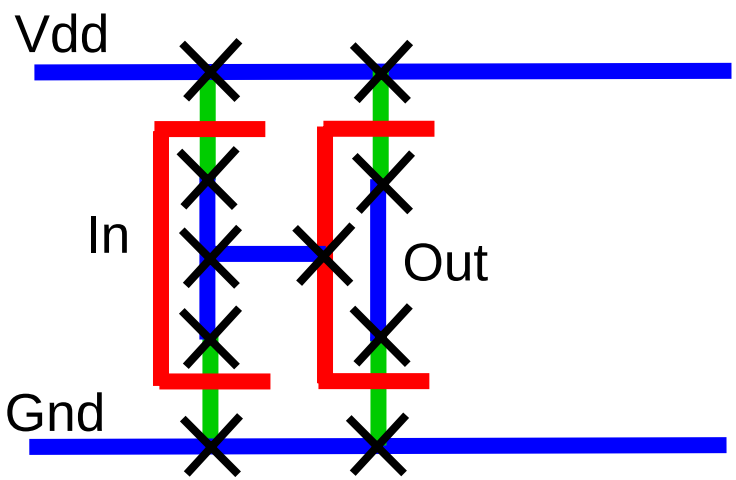


Dual-Well Trench-Isolated CMOS Process

Circuit Under Design

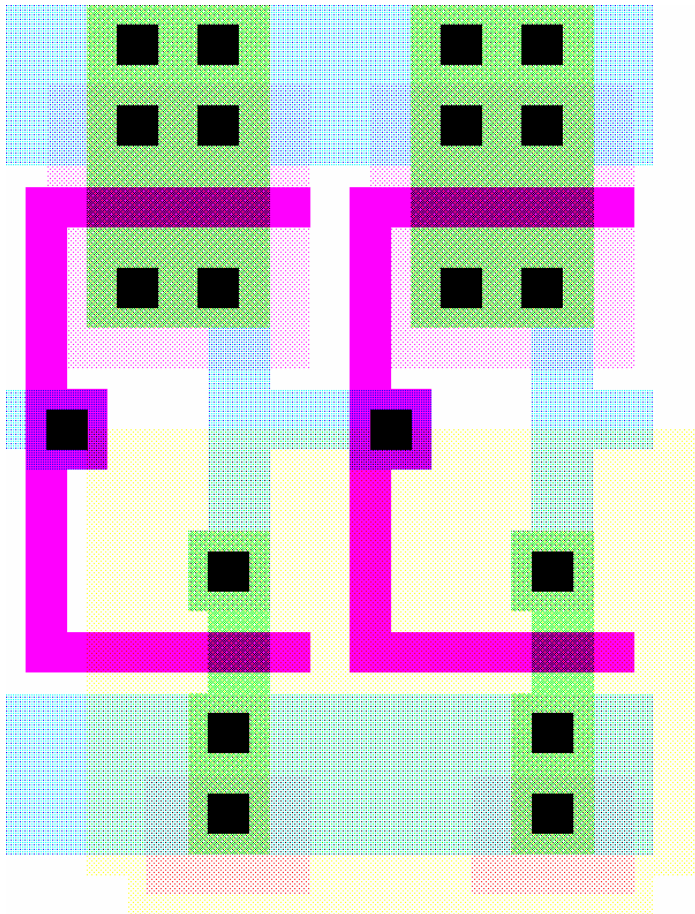


Stick Diagram

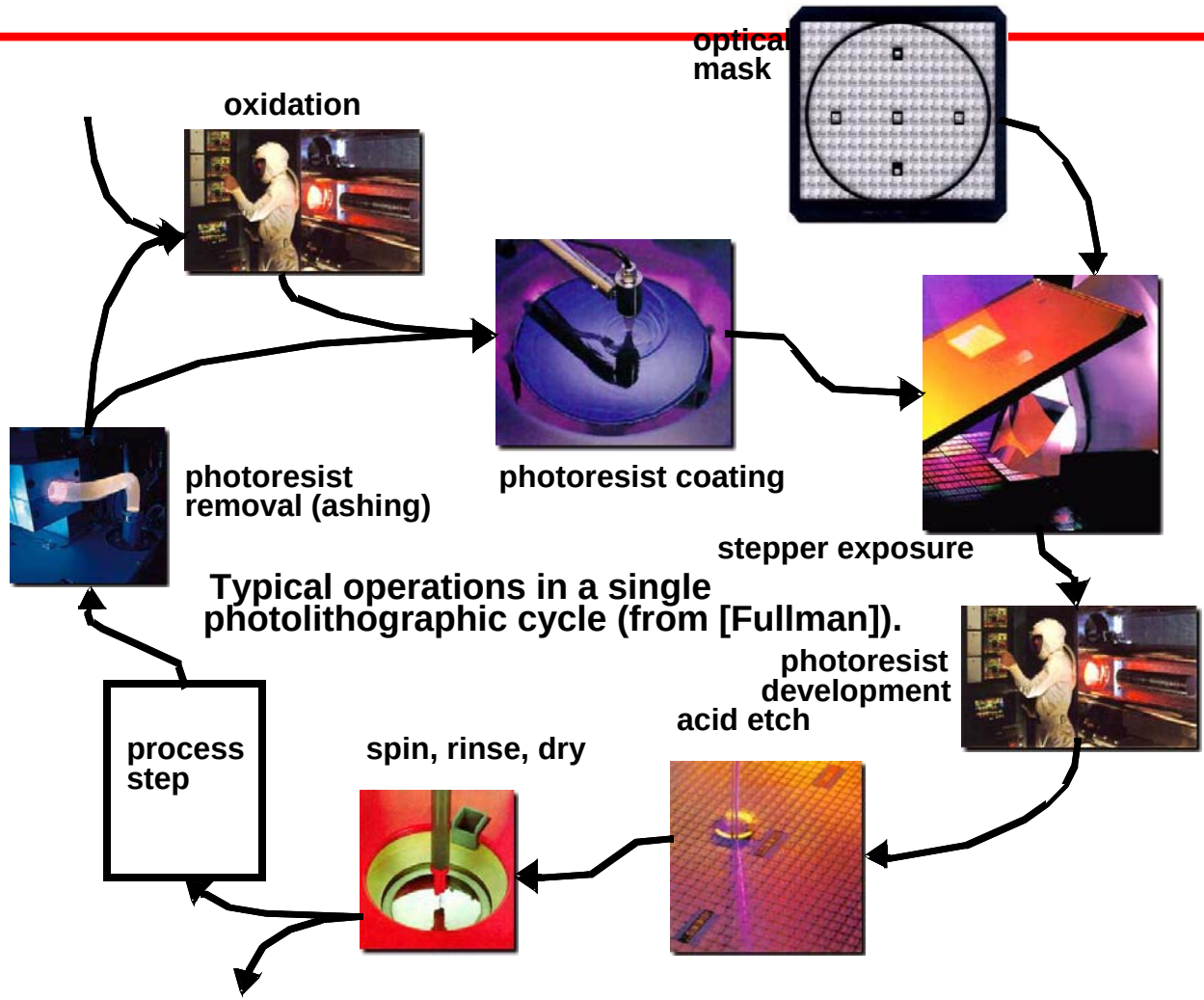


- Useful to visualize the layout you intend to use for a gate
- Color = layer
- X means connected
- Get the topology right first
- Does not have to be this neat
- Buy erasable colored pencils

Its Layout View

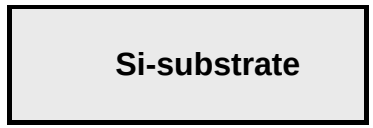


Photolithographic Process

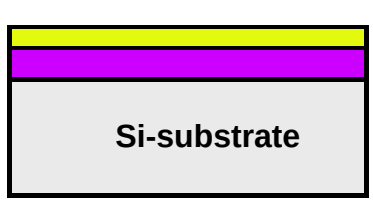


Typical operations in a single photolithographic cycle (from [Fullman]).

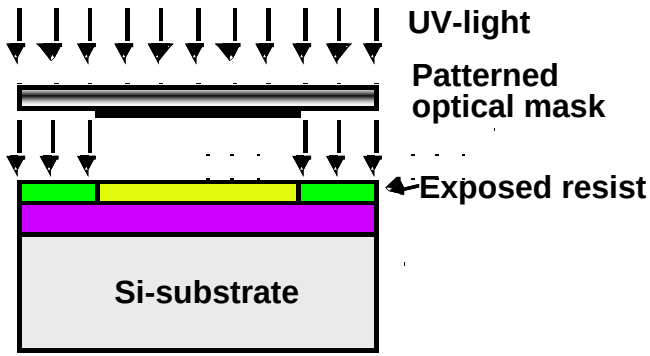
Patterning of SiO_2



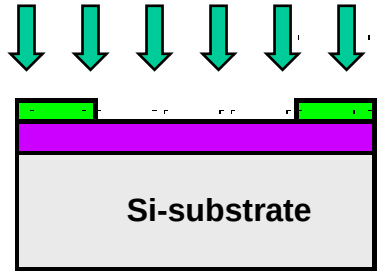
(a) Silicon base material



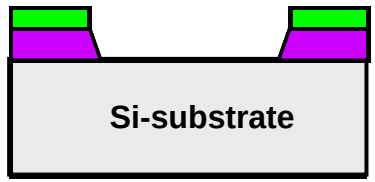
(b) After oxidation and deposition of negative photoresist



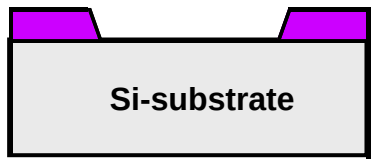
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2

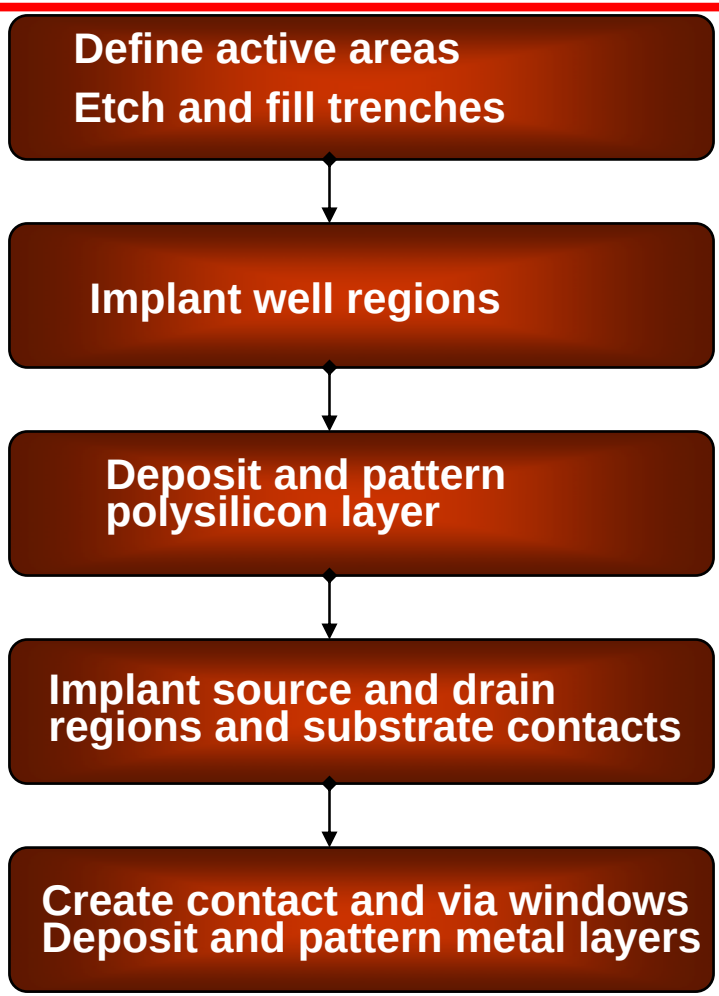


(e) After etching

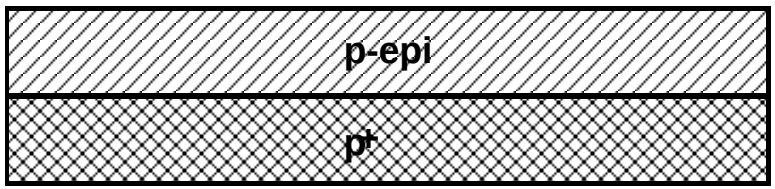


(f) Final result after removal of resist

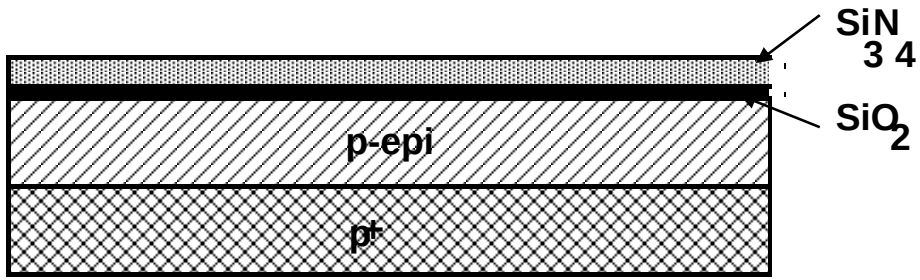
CMOS Process at a Glance



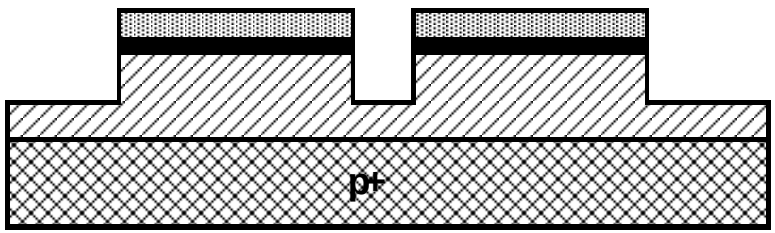
CMOS Process Walkthrough



(a) Base material: p+ substrate with p-epi layer

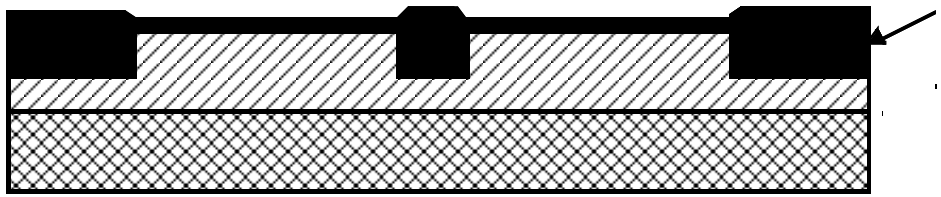


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

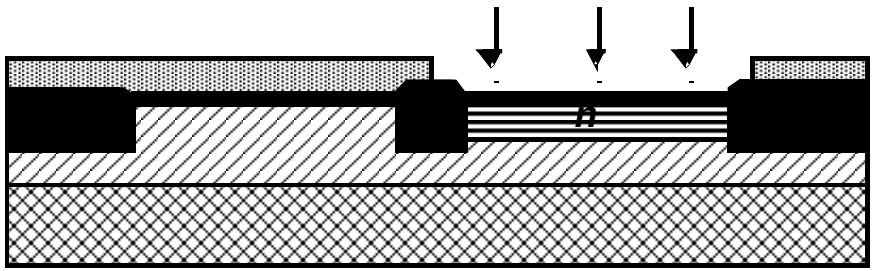


(c) After plasma etch of insulating trenches using the inverse of the active area mask

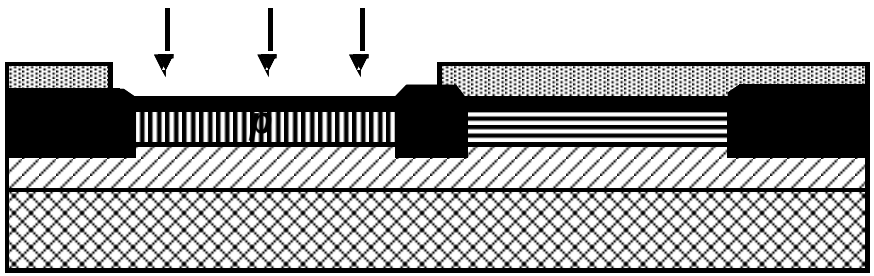
CMOS Process Walkthrough



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

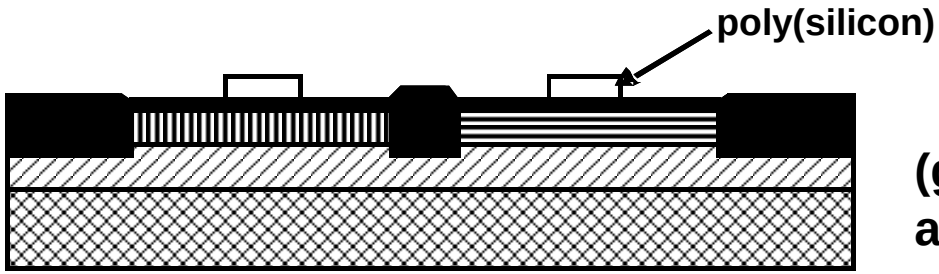


(e) After n-well and Vthp adjust implants

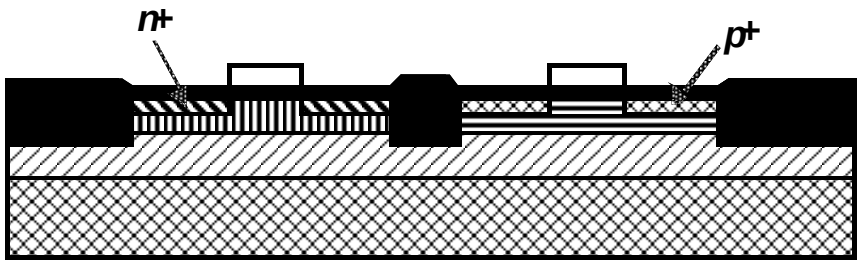


(e) After p-well and Vthn adjust implants

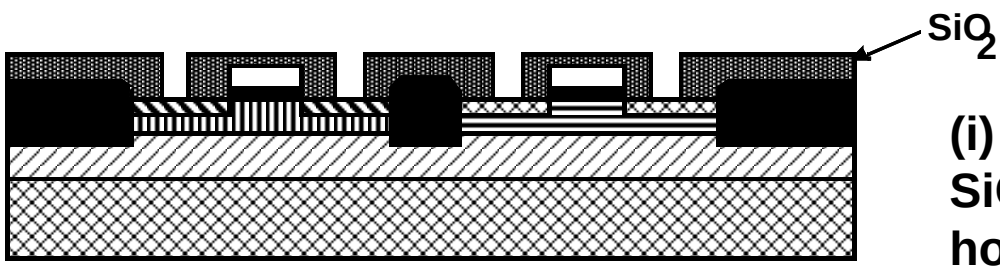
CMOS Process Walkthrough



(g) After polysilicon deposition and etch

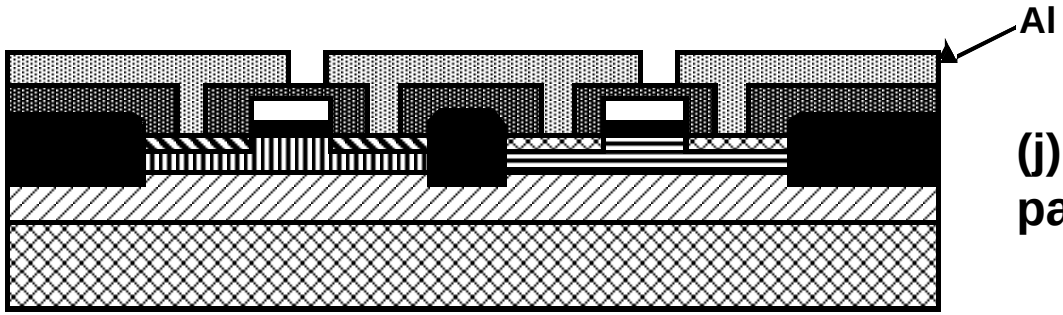


(h) After n+ source/drain and p+ source/drain implants. These steps also dope poly.

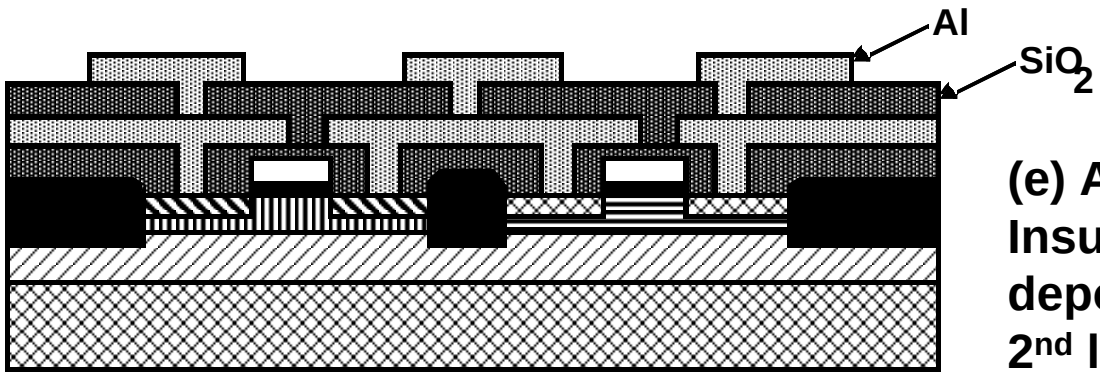


(i) After deposition of SiO2 insulator and contact hole etch

CMOS Process Walkthrough



(j) After deposition and patterning of first Al layer.



(e) After deposition of SiO_2 Insulator, etching of vias, deposition and patterning of 2^{nd} layer of Al

Looking Ahead

- http://jas.eng.buffalo.edu/education/fab/invFab/index.html
- Read Sections 1.1, 1.2, 1.3.2-1.3.4, and 2.2 of Rabaey (mostly review)
- Next lecture: we'll cover design rules and layout styles
- Tutorial Monday 4:00pm & Tuesday at 11:00am
- CAD1 due in 1 week
- HW1 due in 2 weeks
- All will be posted on website soon