EECS 427
Lecture 3: CMOS review II
Reading: 3.1, 3.2, 5.1-5.4, 6.2

Recap

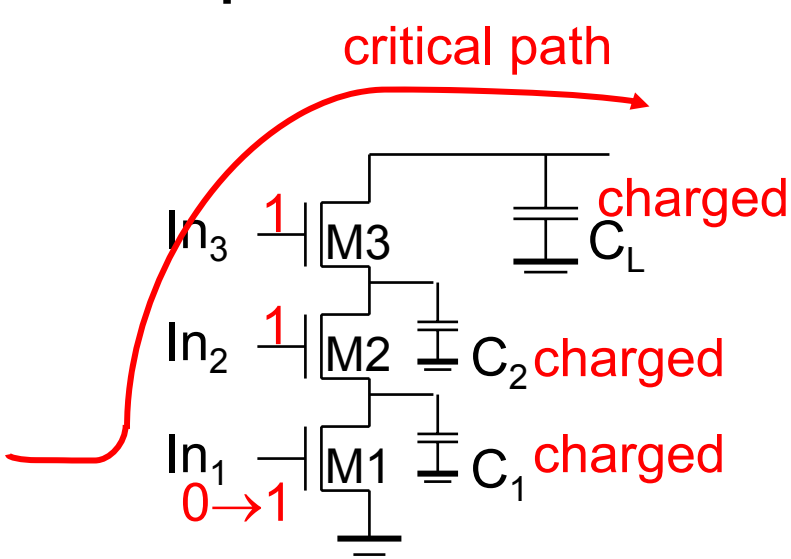
- CMOS review I
  - Basic transistor operation
  - Inverter DC transfer curve
  - CMOS logic driving load capacitance
  - Delay calculation
    - Simplified RC charging/discharging model
    - Dependence of gate size on delay
    - Gate sizing motivation

Outline

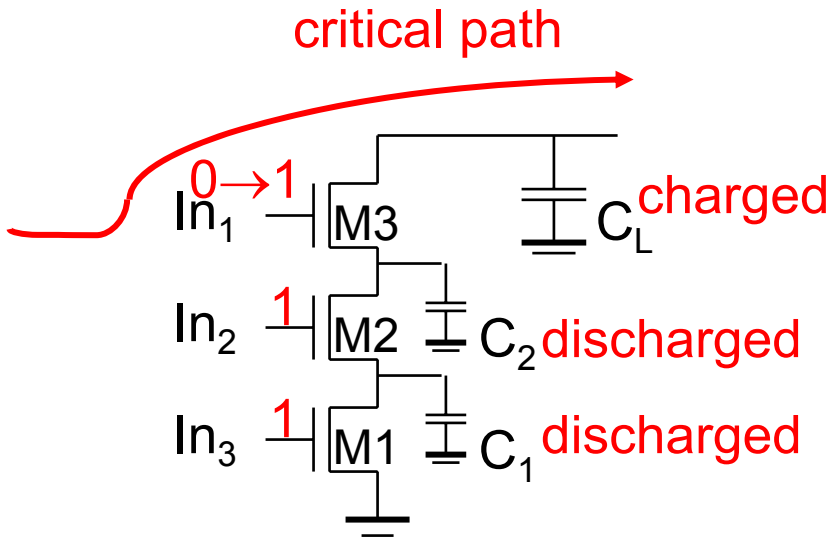
- CMOS review I
  - Basic transistor operation
  - Inverter DC transfer curve
  - CMOS logic driving load capacitance
  - Delay calculation
    - Simplified RC charging/discharging model
    - Dependence of gate size on delay
    - Gate sizing motivation

Fast Complex Gates: Design Techniques

- Transistor ordering to set critical path input closest to output



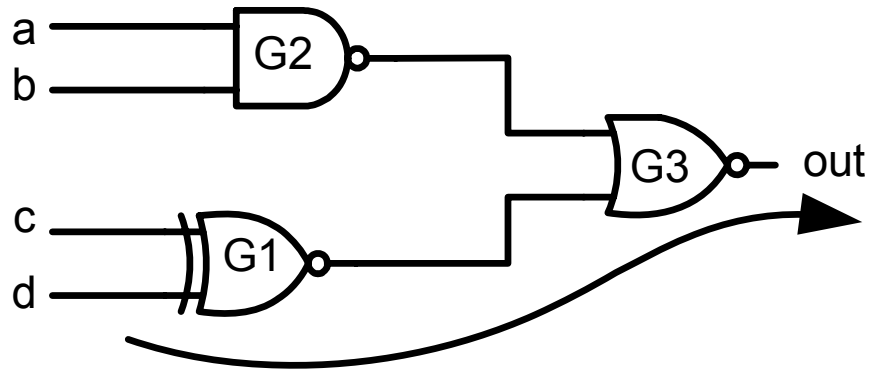
delay determined by time to discharge C_L, C_1 and C_2



delay determined by time to discharge C_L

Fast Complex Gates: Design Techniques- Asymmetric Gates

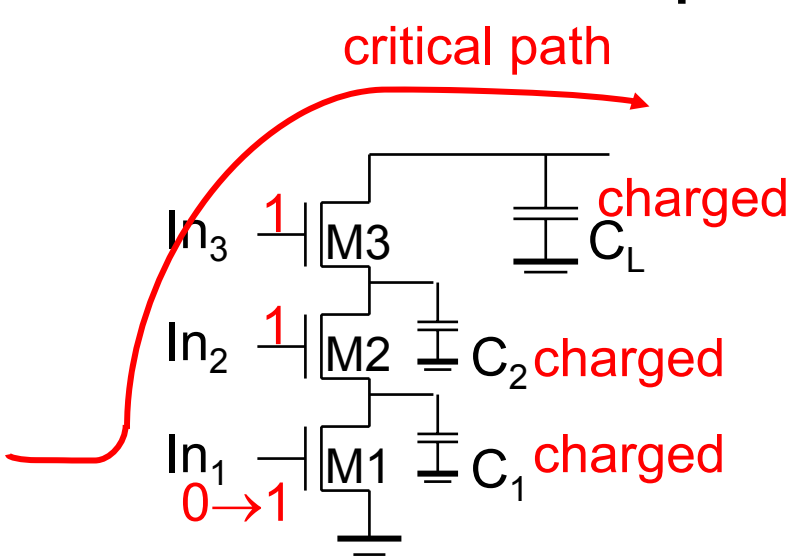
- Critical path is from c/d to output
- Why should gate delay for G3 be equal for both pins?
- Size up one input
  - Increases load capacitance of that pin
  - Improves drive strength of gate



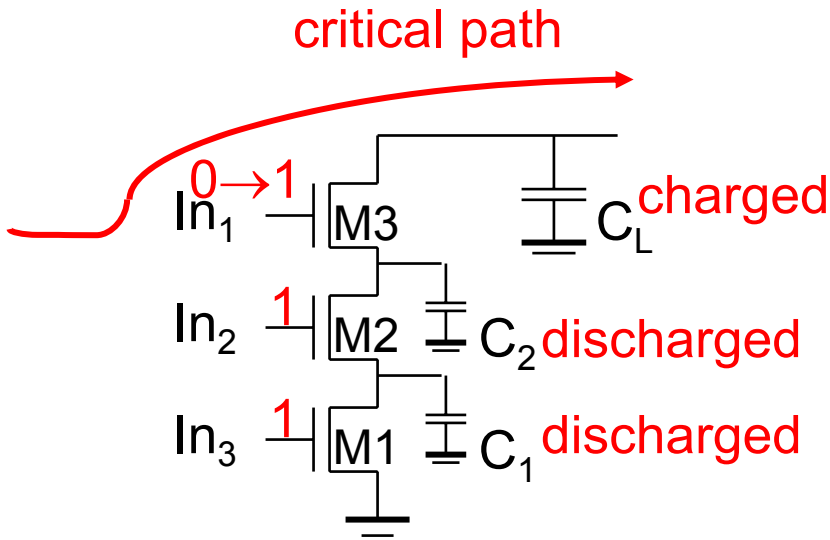
A – out = 100ps
B – out = 120ps
C – out = 200ps
D – out = 200ps

Fast Complex Gates: Pin - ordering

- Pin corresponding to critical path nearest to output



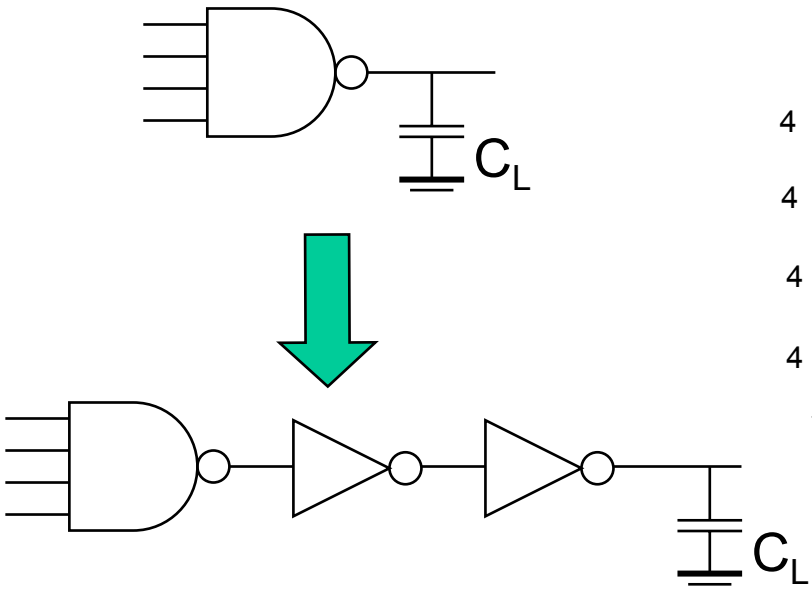
delay determined by time to discharge C_L, C_1 and C_2



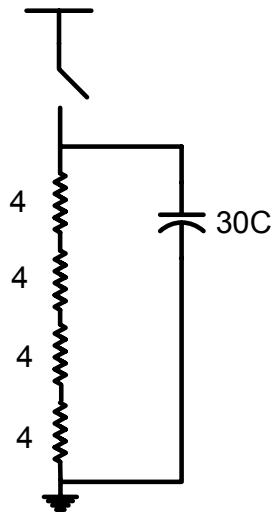
delay determined by time to discharge C_L

Fast Complex Gates: Design Techniques

- Isolating fan-in from fan-out using buffer insertion

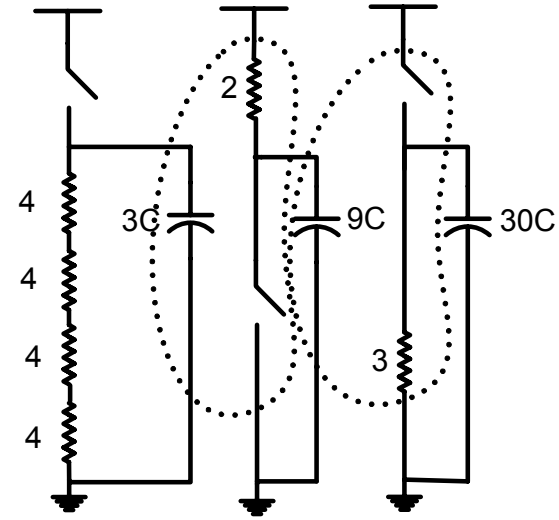


τ = 1R . 30C



VS.

τ = 1R . 3C + 1R * 9C + 1/3R * 30C = 22RC



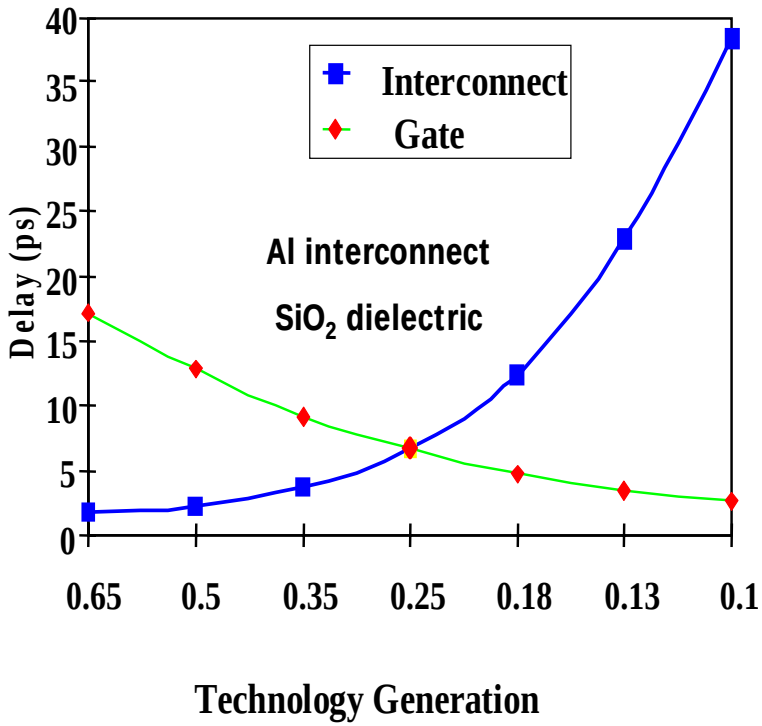
Let 1 width unit have 1C of load capacitance, assume □ = 2

Recommended evaluations

- Calculate the β ratio in your process
- Compute I_{dsat} and V_{dsat} for NMOS and PMOS devices
- Calculate the approximate gate capacitance per micron for NMOS and PMOS devices
- Calculate unit inverter delay (Wn=1u, Wp= for: β u
  - Self-loading
  - 10 micron of M1 wire with adjacent metal
  - Driving 4 copies of itself

Interconnect

- Gate delays reduce with technology scaling
- Global interconnect delays increase with scaling
  - Interconnects must be included in analysis and optimization



Interconnect Parasitics

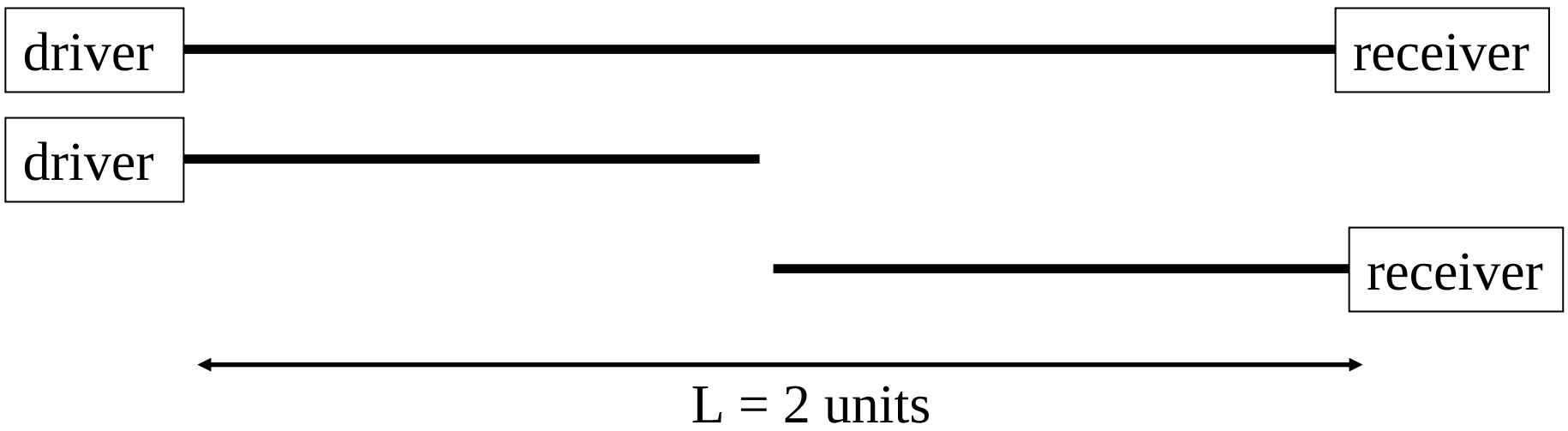
- Classes of parasitics
  - Capacitance
  - Resistance
  - Inductance (627 focuses on this)
- Impact of interconnect parasitics
  - Increases propagation delay
  - Energy dissipation
  - Loss in power distribution
  - Reliability and signal integrity
  - Clock-skew

Interconnect Modeling

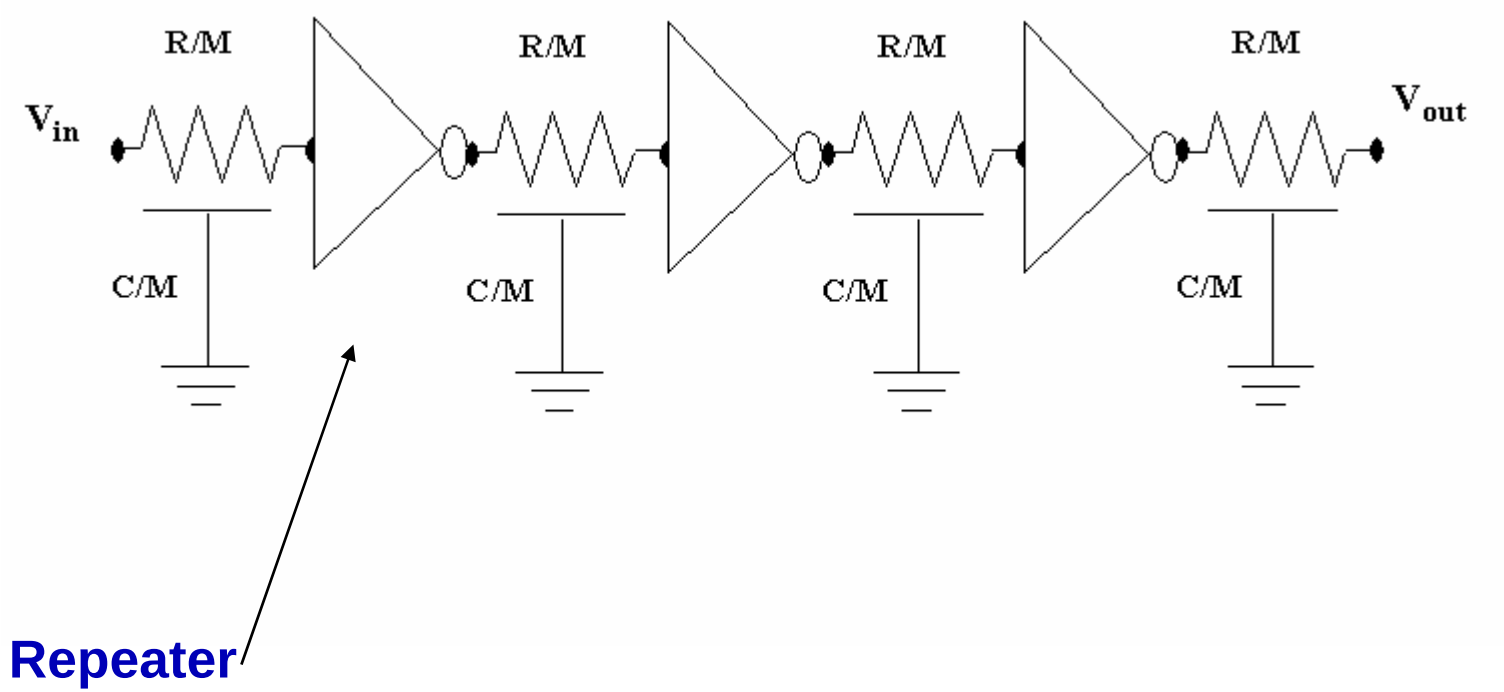
- Lumped capacitance model is what we use for device/gate analysis
- Lumped RC model
  - For simple one segment RC:
    - 50% Delay = 0.69*RC
    - 10-90% Slew = 2.2*RC
- Distributed RC line model
  - More accurate for interconnect analysis
    - 50% Delay = 0.38*RC
    - 10-90% Slew = 0.9*RC
- Either way, wire delay is quadratic with wire length

How to reduce RC delay

- Since RC delay is quadratic with length, reducing length is key
- Note: $2^2 = 4$ and $1+1 = 2$ but $1^2 + 1^2 = 2$



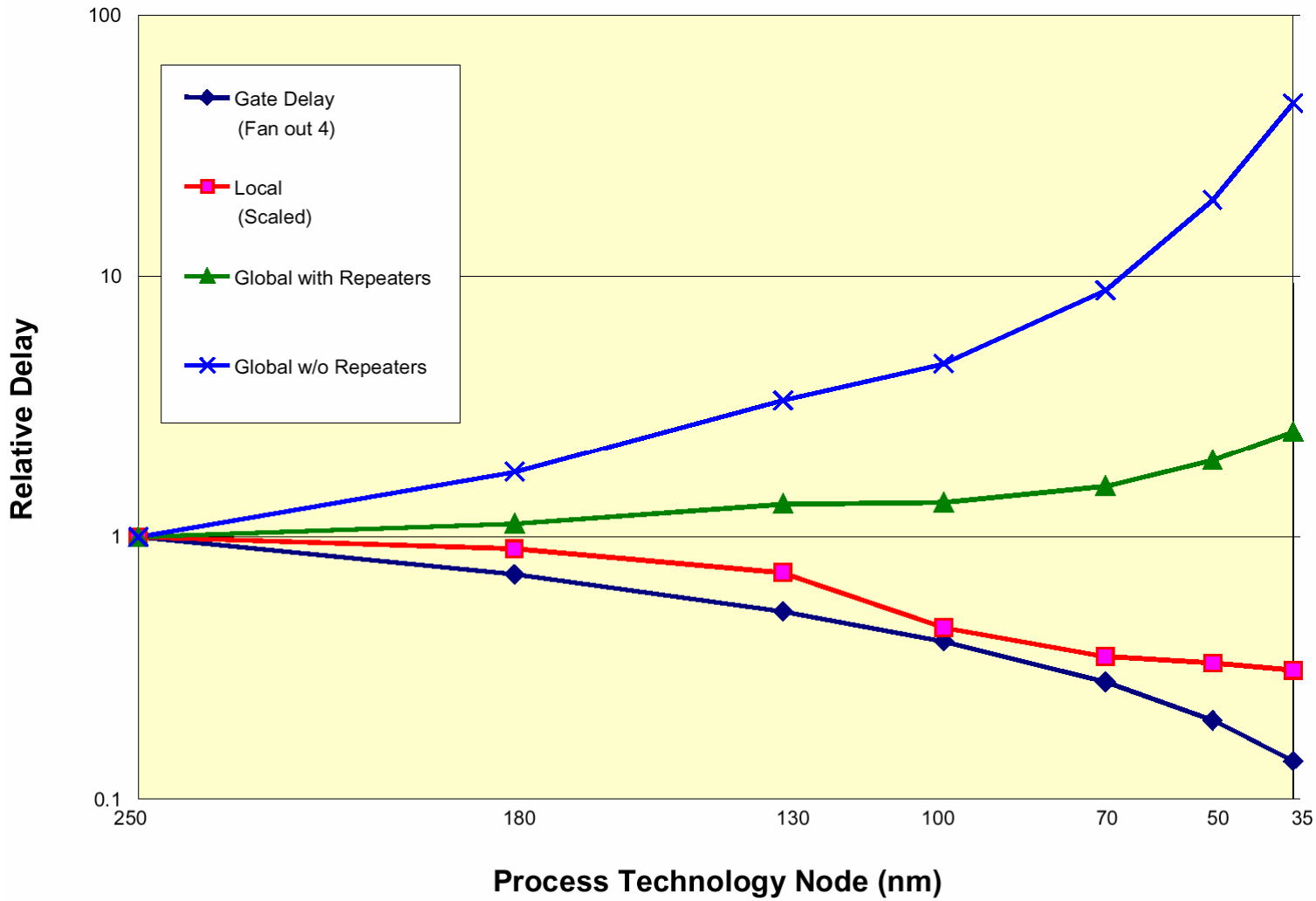
Repeaters



Repeater = strong driver (usually an inverter or pair of inverters for non-inverting polarity) placed along a long RC line to “break up” the line and reduce delay

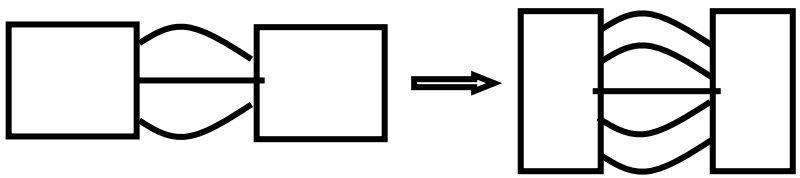
We need to determine optimal # of repeaters and their size based on wire and device delay properties

Repeaters Impact

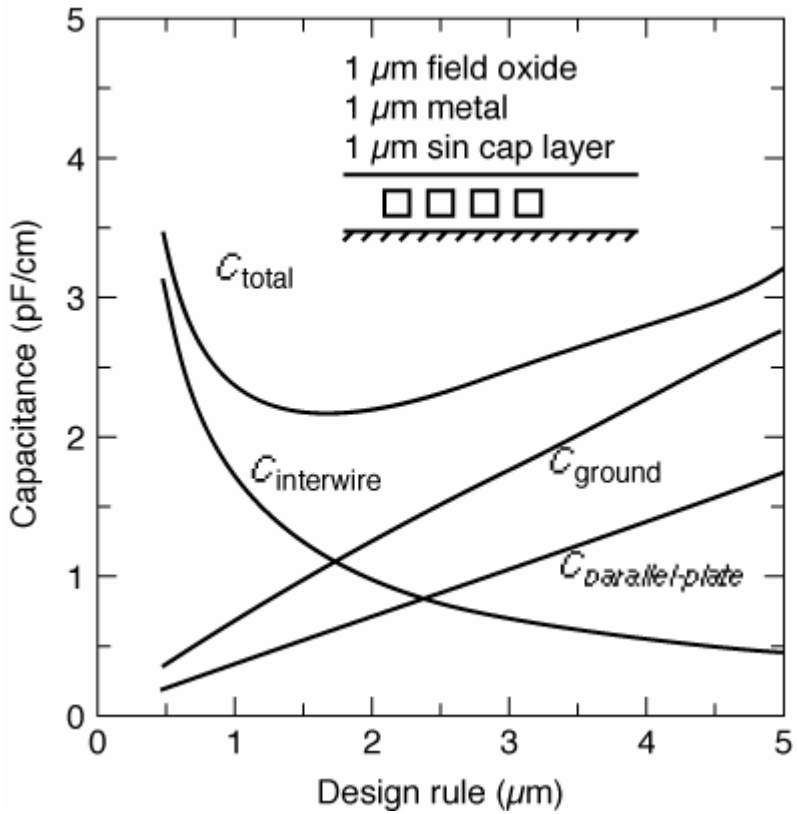


Coupling Capacitance

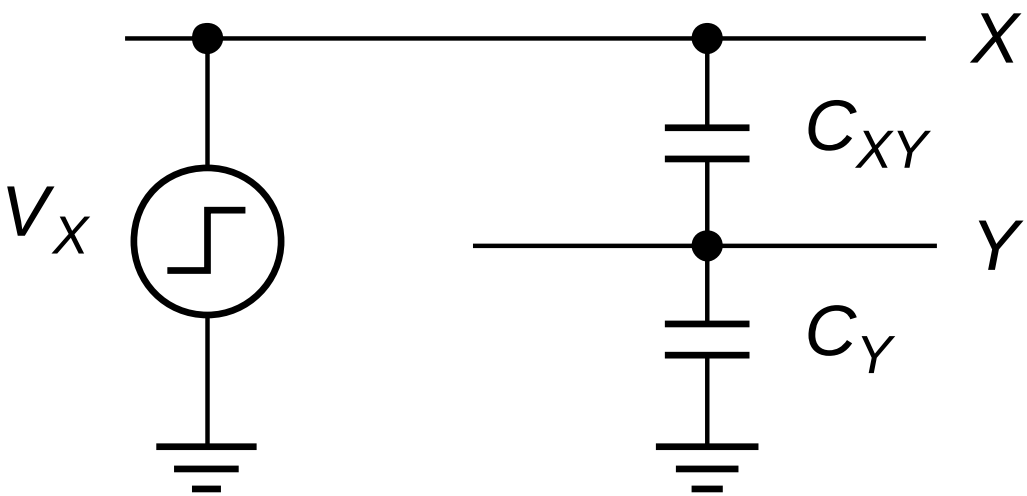
- To reduce interconnect resistance, thickness is not scaled as aggressively as the width of the interconnect



- Tall wires (high aspect ratios)

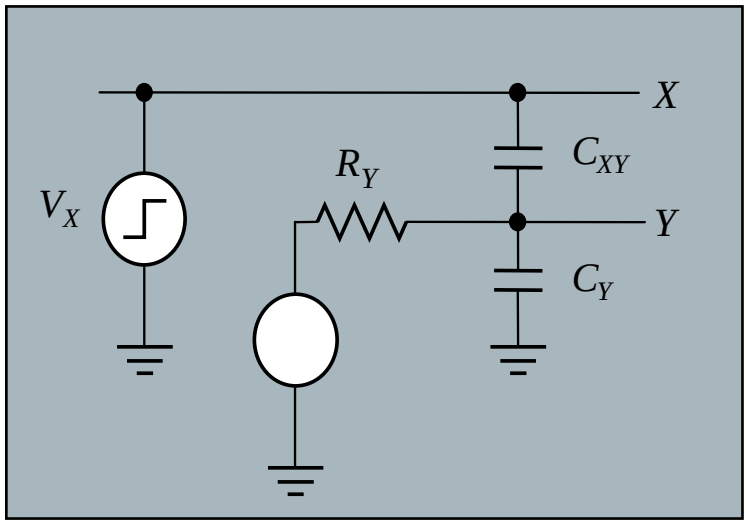


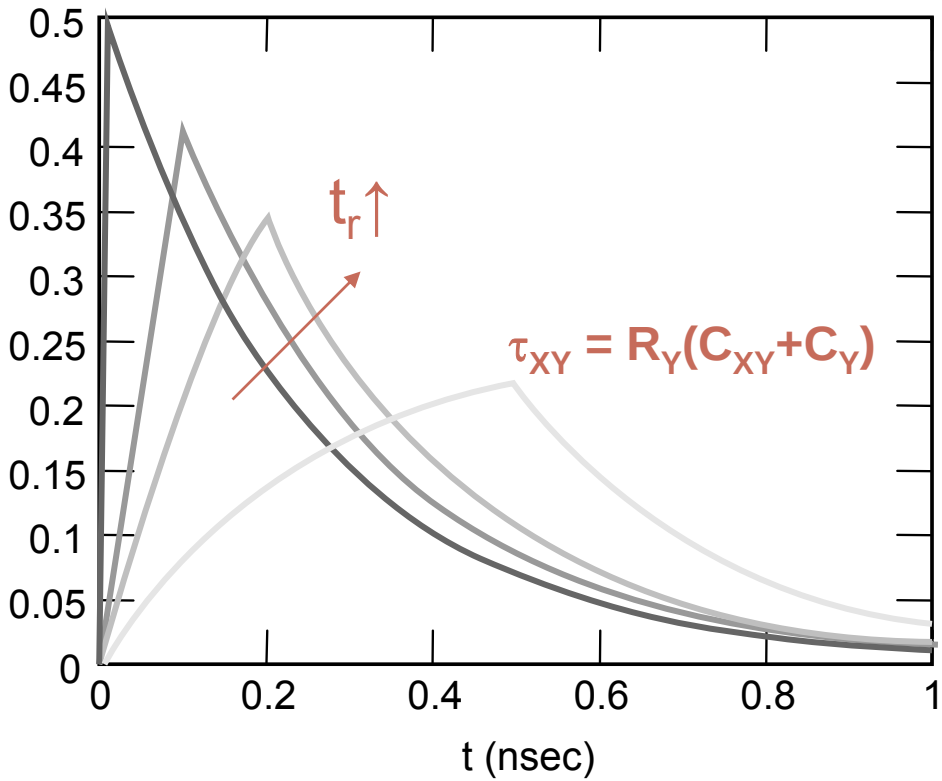
Capacitive Cross Talk



$$\Delta V_Y = \frac{C_{XY}}{C_Y + C_{XY}} \Delta V_X$$

Capacitive Cross Talk



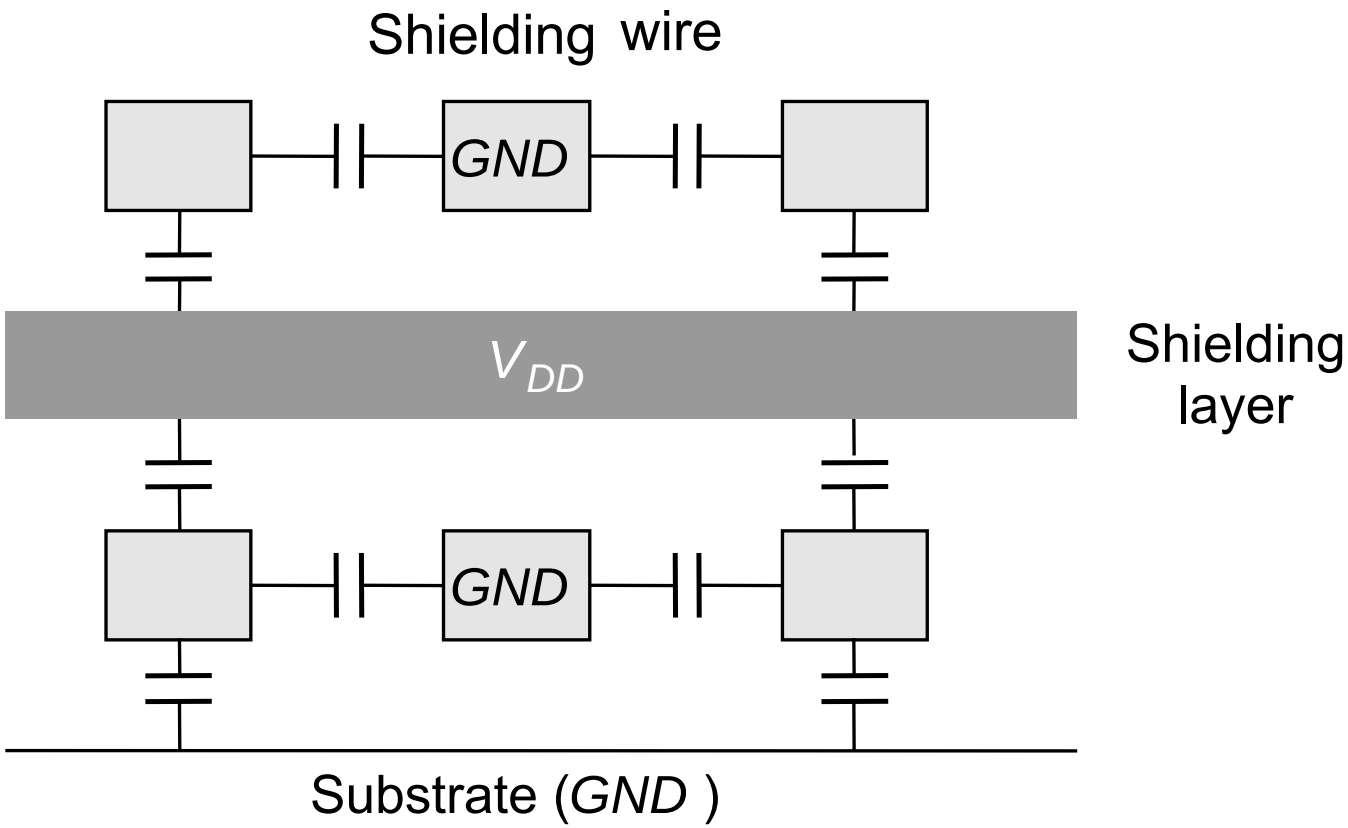


Keep time-constant small (size up driver of node Y)

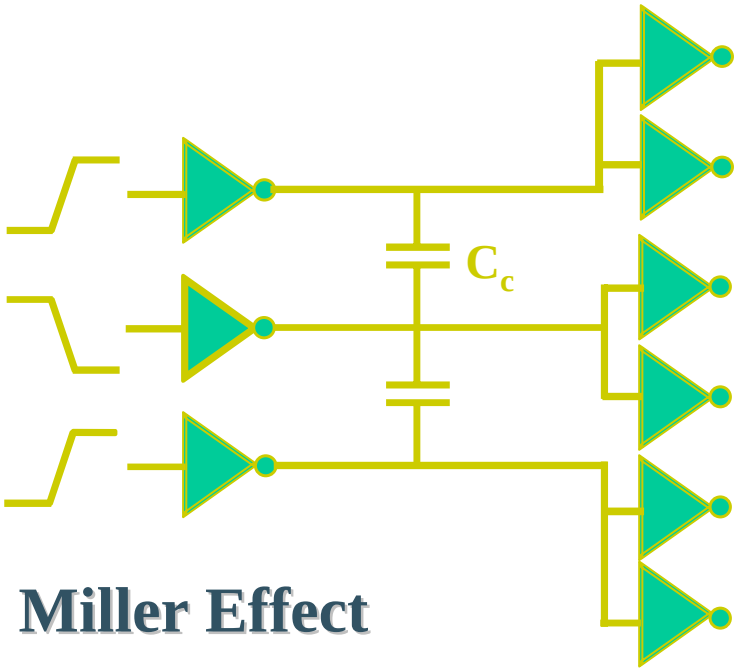
Dealing with Capacitive Cross Talk

- Avoid floating nodes (keepers!)
- Protect sensitive nodes (keep wires short)
- Make rise and fall times as large as possible
- Do not run wires together for a long distance
- Use shielding wires
- Use shielding layers

Shielding



Impact of Crosstalk on Delay



Miller Effect

DELAY DEPENDENT UPON ACTIVITY IN NEIGHBORING WIRES! (very important today)

- Both terminals of capacitor are switched in opposite directions
  $(0 \rightarrow V_{dd}, V_{dd} \rightarrow 0)$
- Effective voltage is doubled and additional charge is needed (from Q=CV)