EECS 427
Lecture 4: Euler Path layout, Registers
Reading: Insert D, 7.1, 7.2

Last Time

- Static CMOS review
  - No static power dissipation
  - Full logic swing
  - Easy to design, non-ratioed
  - Delay analysis
  - Sizing of gates

Today

- The Euler path layout method
- Registers & timing review
- Project Group getting to know everyone

Euler Path Layout

- Semi-automated way to share sources, drains
- Can be a useful tool to get you started
- Not always the best approach
- Know Euler's results, makes things much easier
  - Odd degree vertices are problems
  - If two such vertices, start at one end at other.

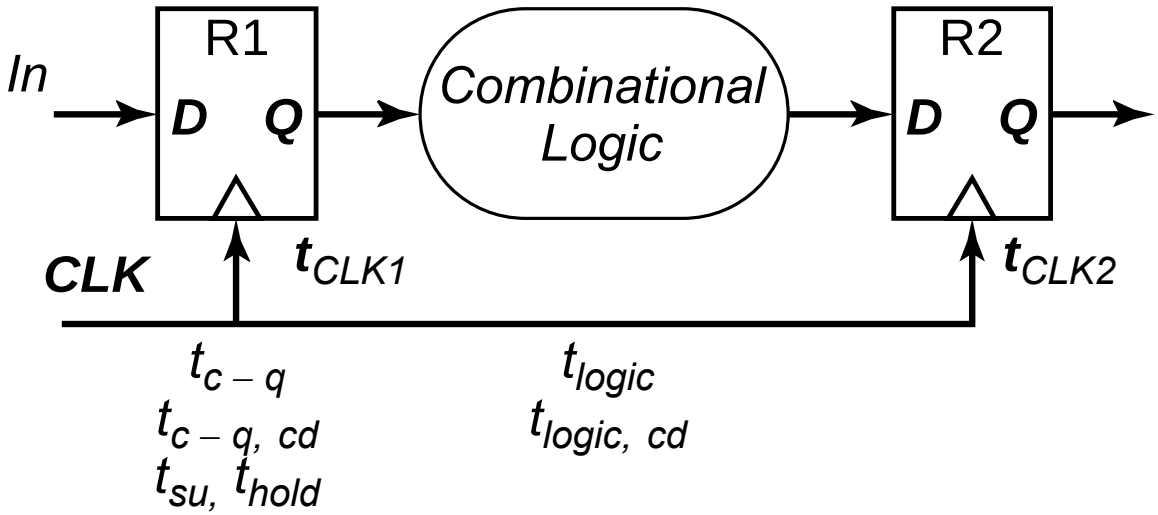
Euler Path Layout

- Two graphs: pmos, nmos
- Vertices are nets (source/drain)
- Edges are gates (also nets)
- Walk two simultaneous Euler paths through graphs hitting edges with same label whenever possible
- Draw paths as lines, label, connect and you have a stick diagram of a layout

Quick Flip-Flop (Register) Discussion, CAD2

- Clocked inverters vs. transmission gates vs. nand gates
- Weak inverters
- Asynchronous reset options
- Bitslice width matching
  - Diff. components of datapath should align (see document on web)

Timing Constraints

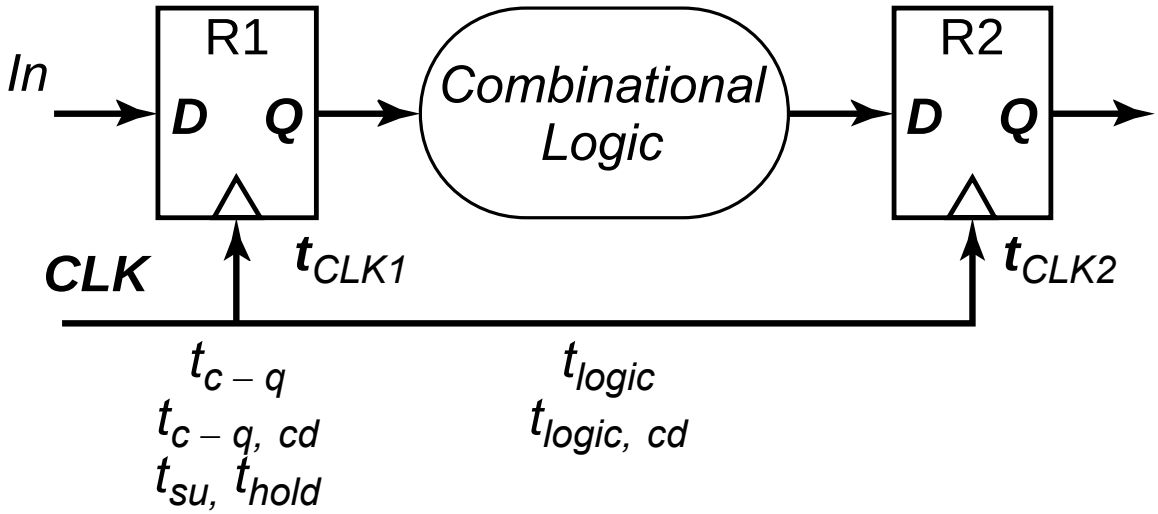


Minimum cycle time:

$T \geq t_{c\text{-}q} + t_{su} + t_{logic} - \delta$

Worst case is when receiving edge arrives early (negative δ)

Timing Constraints



Hold time constraint:

$$t_{(c\text{-}q,\ cd)} + t_{(logic,\ cd)} > t_{hold} + \delta$$

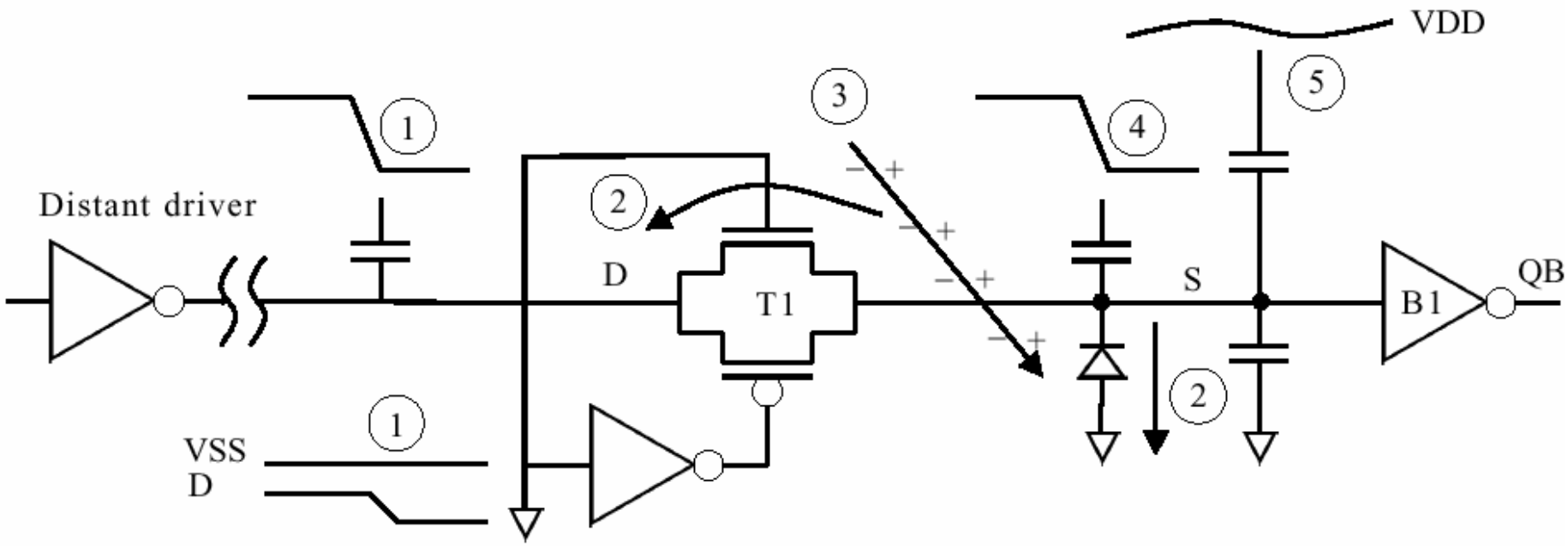
Worst case is when receiving edge arrives late (positive skew)
Race between data and clock
cd: contamination delay (fastest possible delay)

Requirements in Flip-Flop Design

- High speed:
  - Small Clk-Output delay
  - Small setup time
  - Small hold time→Inherent race immunity
- Low power
- Small clock load (clock power is very large)
- High driving capability
- Integration of the logic into flip-flop
- Multiplexed or clock scan (testability)
- Robustness
- Crosstalk insensitivity
  - Dynamic/high impedance nodes are affected

Sources of Noise

1. Noise on input
2. Leakage
3. α-Particle and cosmic rays
4. Unrelated signal coupling
5. Power supply ripple



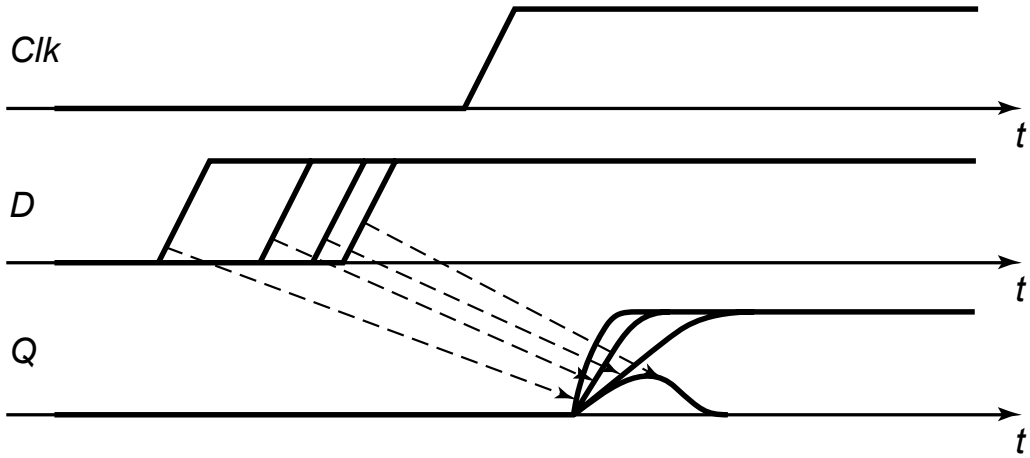
Flip-Flop Robustness

- Input isolation
  - Don’t use a pass-transistor directly at the input (use a buffer)

Storage node related issues:

- Robustness
  - No floating nodes, create pseudo-static storage nodes
- Min capacitance limit
  - Storage node (middle of cross-couple) should have a decent amount of capacitance for noise immunity
  - Too much will slow things down though…
- Preventing exposure
  - Wires associated with storage node should be short, suppress possible coupling to other nodes

More Precise Setup Time Definition

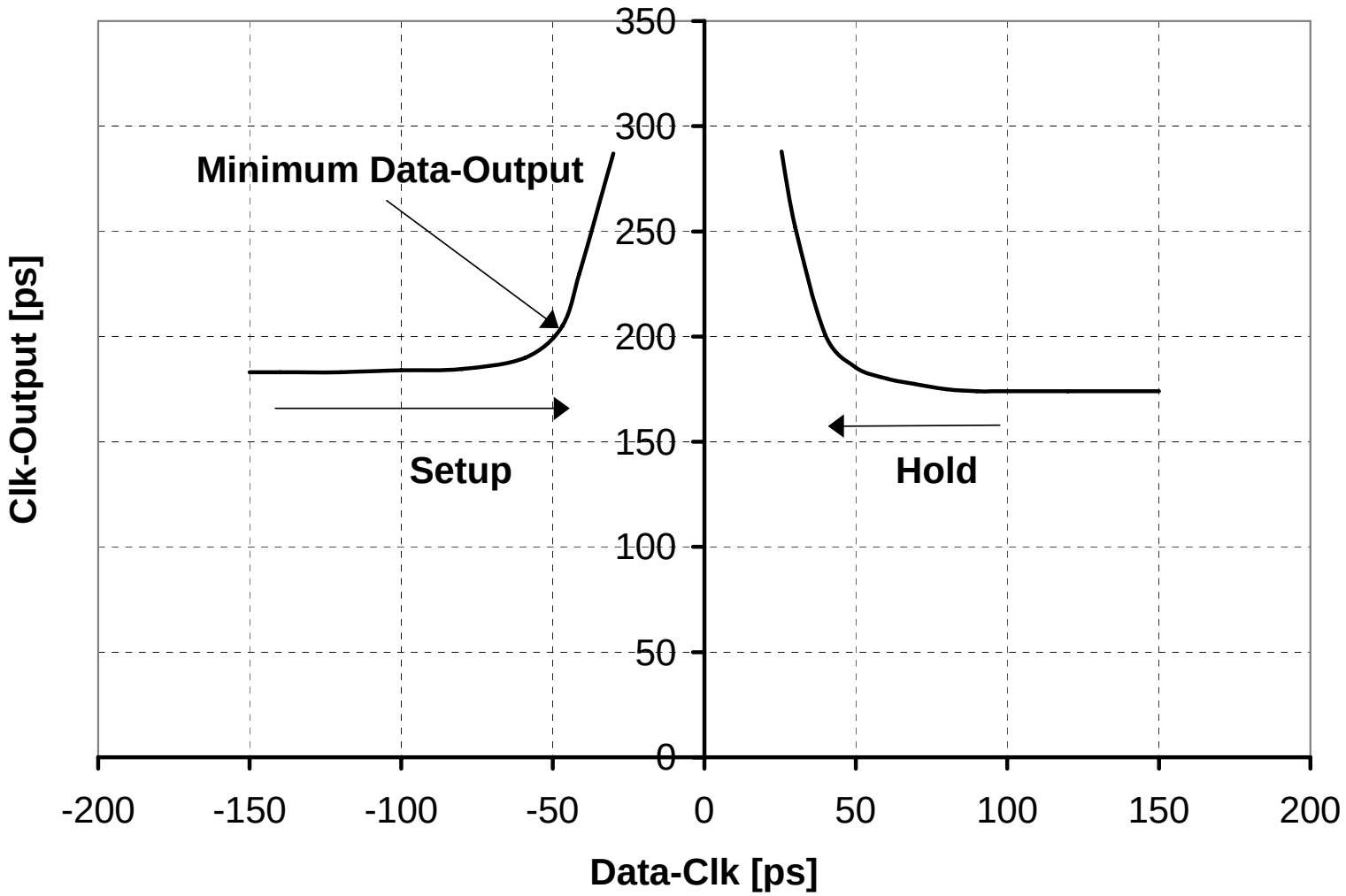


Setup time is a fairly vague concept

- The correct data can be captured but the delay can be greatly affected
- Where is the threshold?

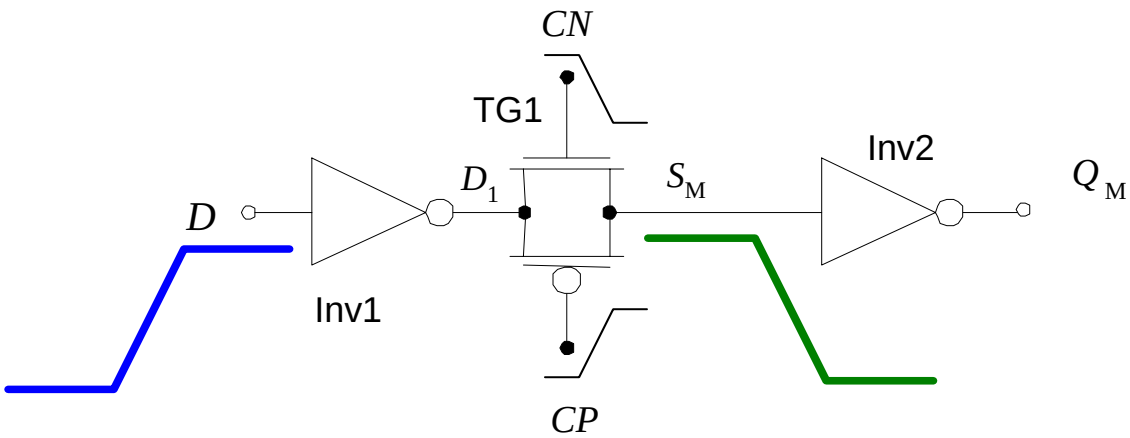
Minimum D-Q delay is the fastest possible way to transfer input to output, related to the sum of T_{setup} and T_{clk-Q}

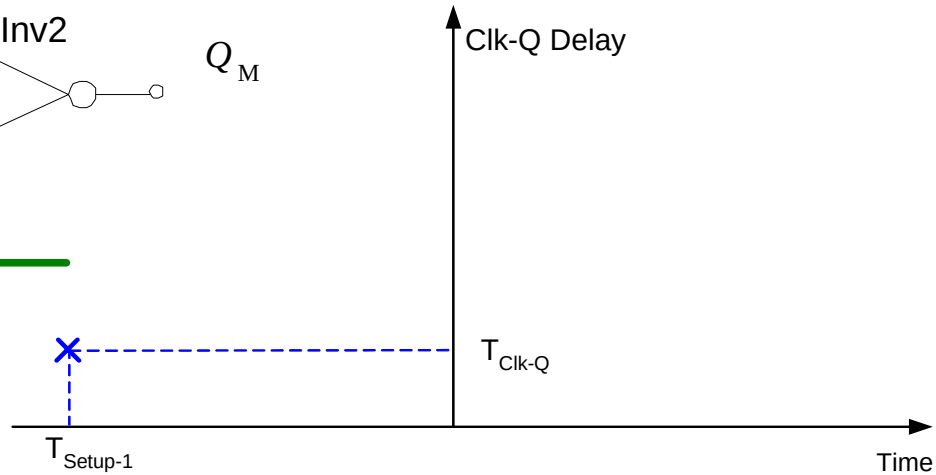
CLK-Q vs. Setup/Hold Times

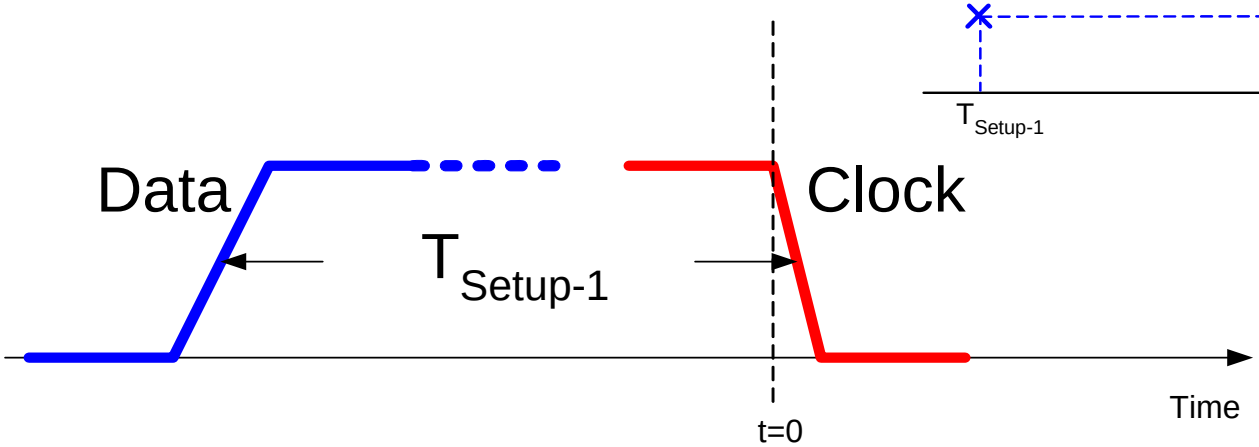


Setup Time Illustrations

Circuit before clock arrival (Setup-1 case)







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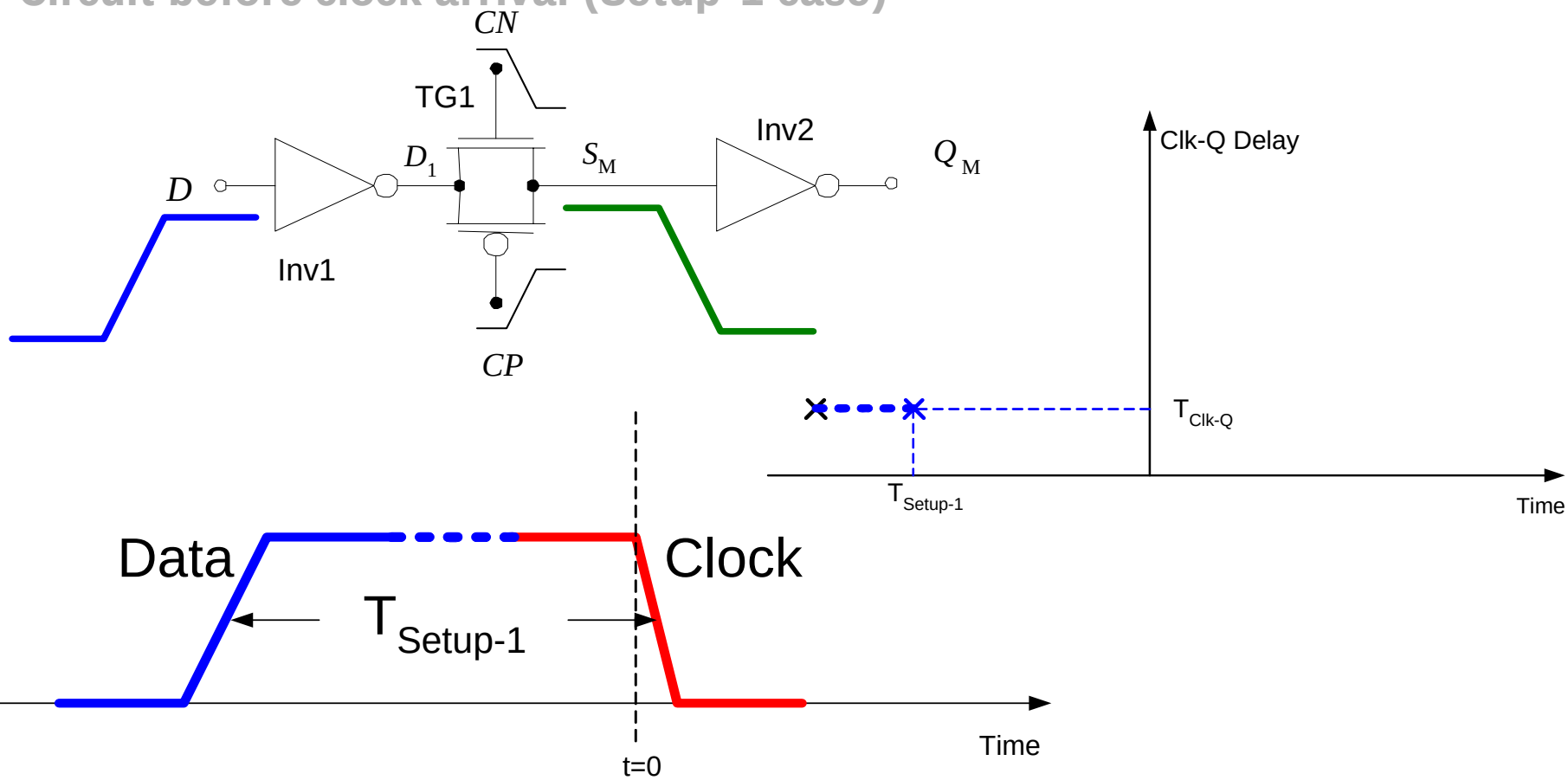

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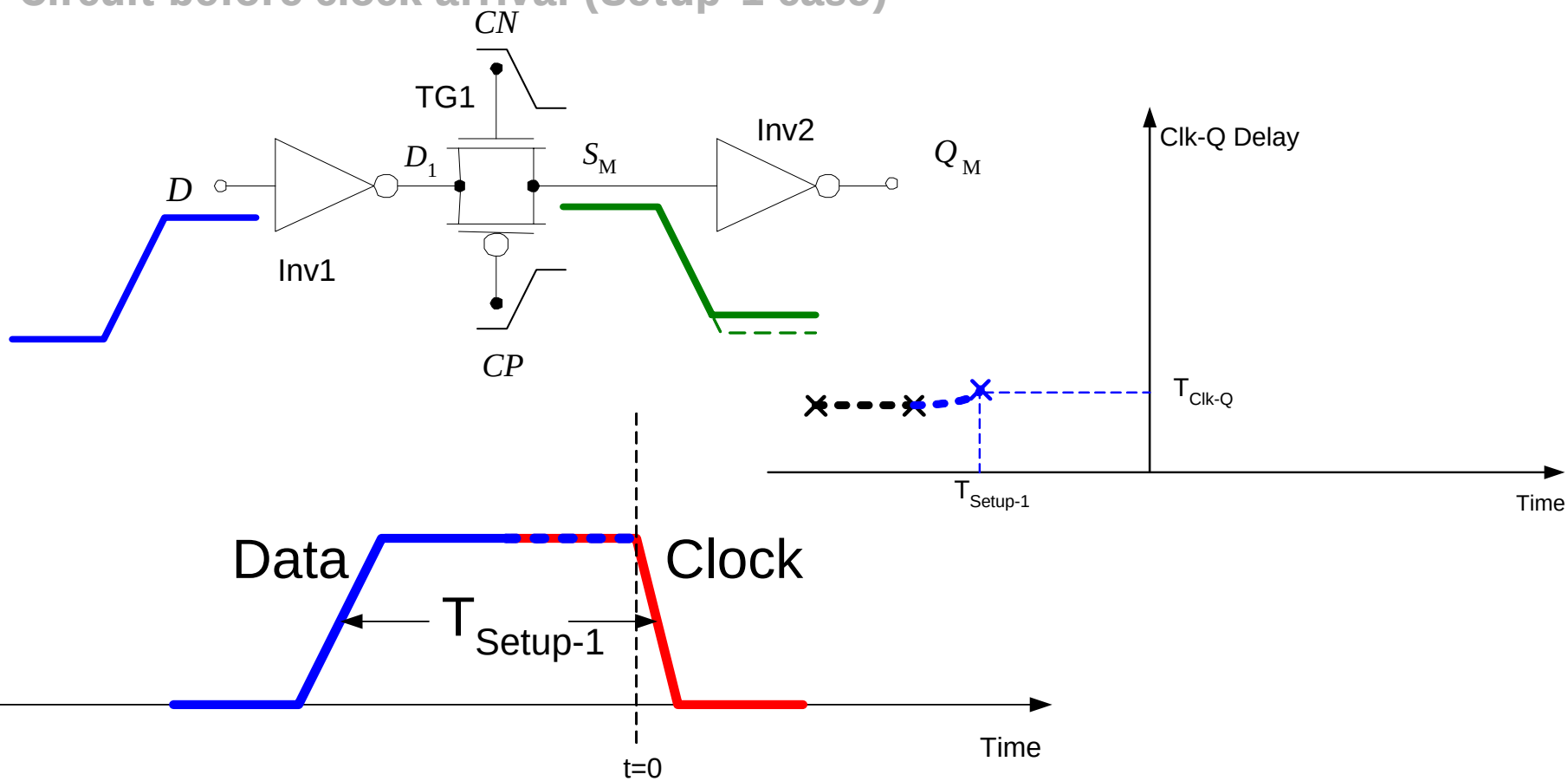

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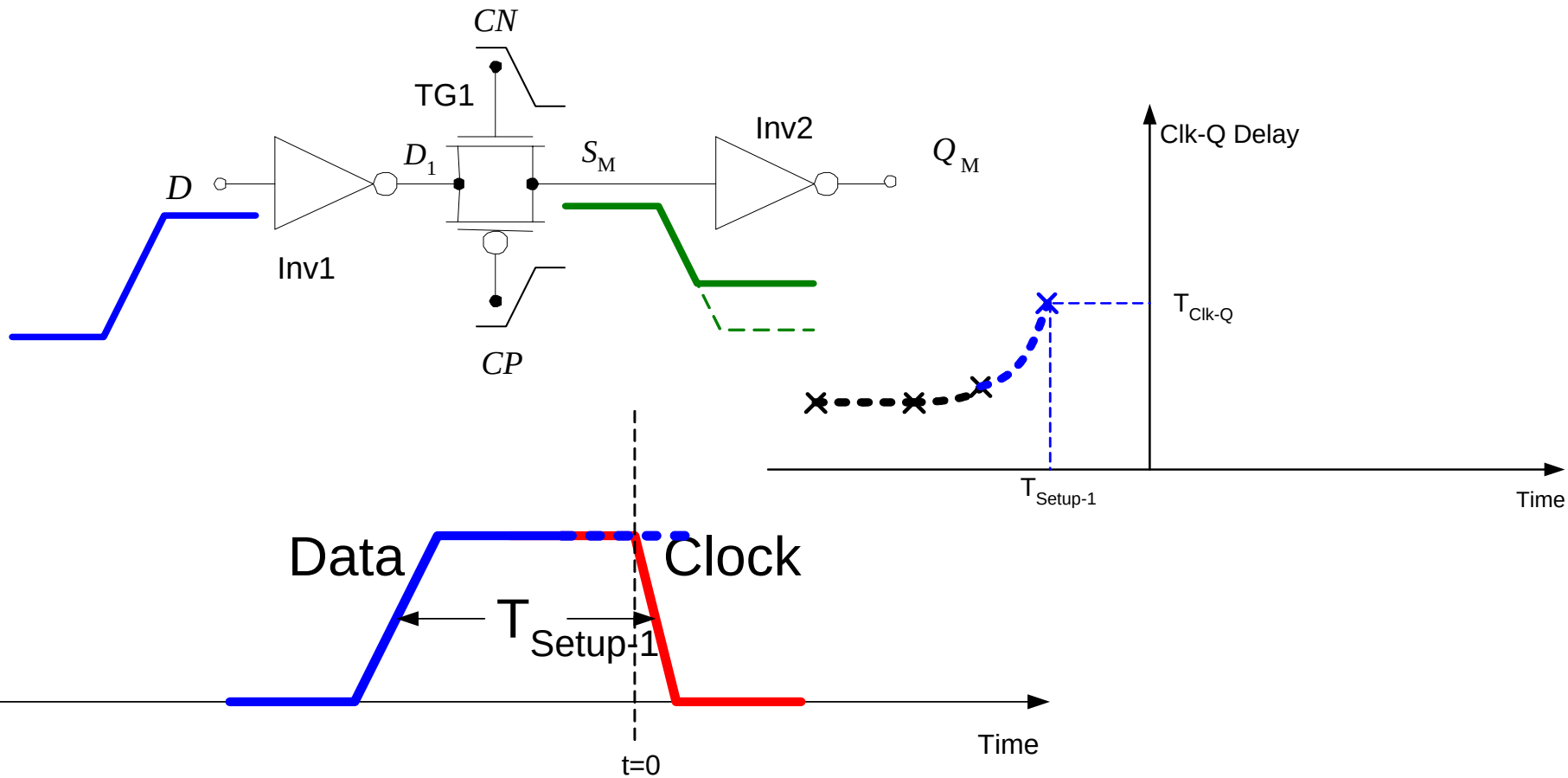

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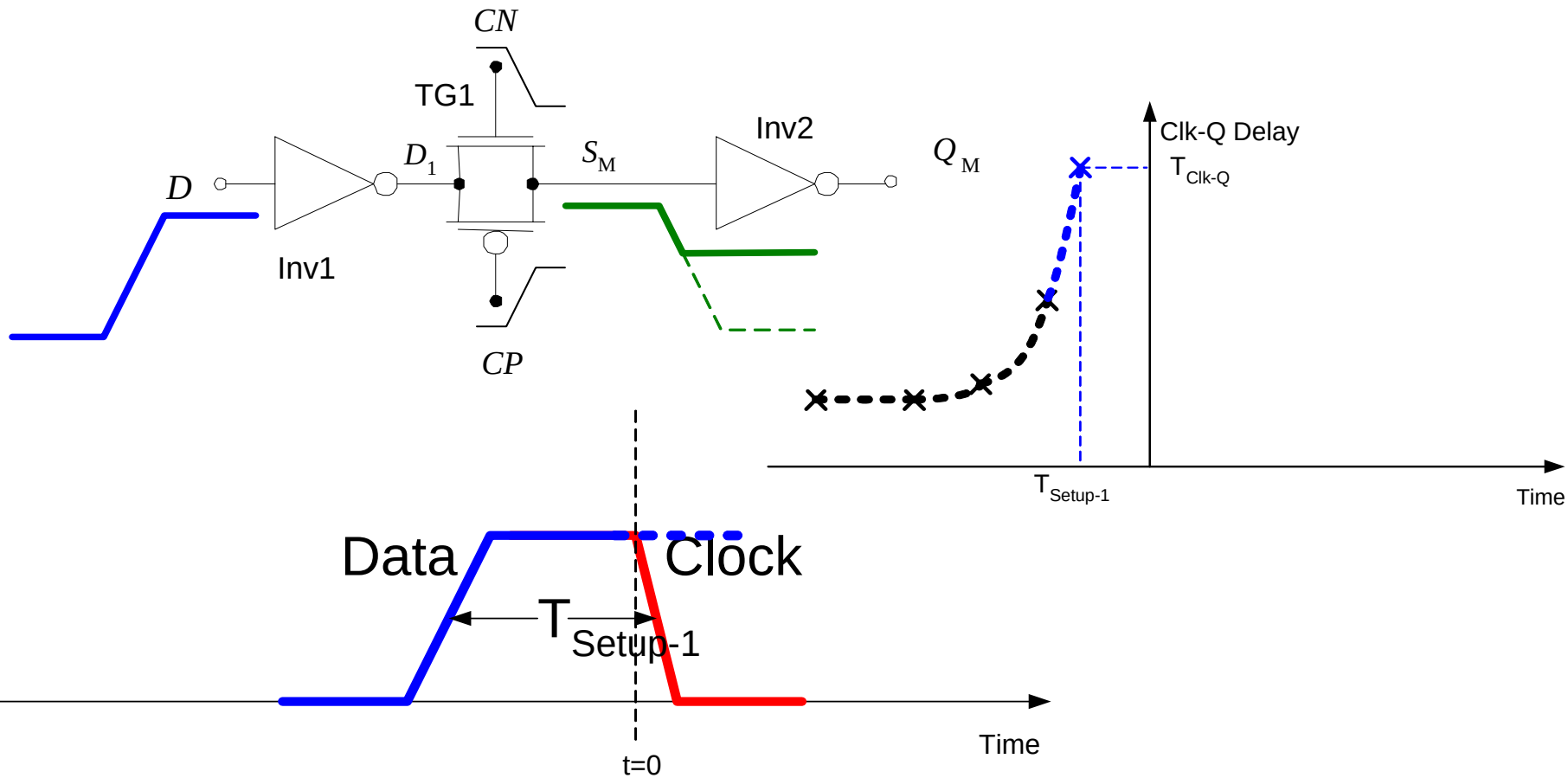


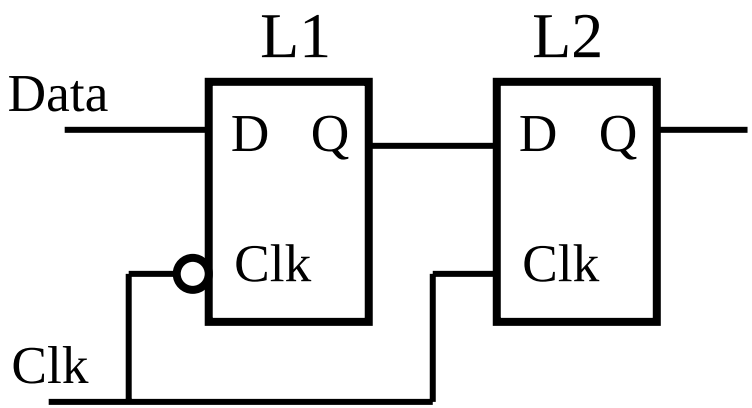
D-Q and setup time summary

- Define setup time as the point at which CLK-Q delay rises 5% beyond nominal
  - Nominal is measured when data arrives much earlier than CLK edge
  - This corresponds roughly to where the total D-Q delay is minimized

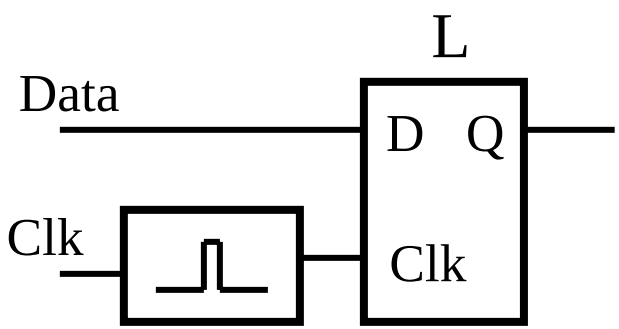
Pulse-Triggered Registers
An Alternative Approach

Ways to design an edge-triggered sequential cell:

Master-Slave Latches



Pulse-Triggered Latch



CAD 2

- Don’t worry too much about sizing
- Try not to be penny-wise and pound-foolish
- The best way to a small layout is have fewer transistors to lay out
- Control signals generally shared, think about part as one in a row of similarly controlled cells

Forming Groups

- Want:
  - Good layout
  - Good logic synthesis
  - Understand of architecture
  - An application and knowledge of it
  - Reasonably similar aspirations for the project
  - Personal compatibility