EECS 427
Lecture 6: Logic Effort
Back of the envelope gate sizing

Reading : Sutherland et. Al “Logical Effort”

Outline: logic effort

- Motivation and intuition
- Model the delay of one gate
- The delay of a chain of gates (multistage)
- Branching
- Minimum delay
- Best number of stages and gate sizing
- Complex gates
- Asymmetric gates
- Unequal rise and fall times
- Examples
- Limitations

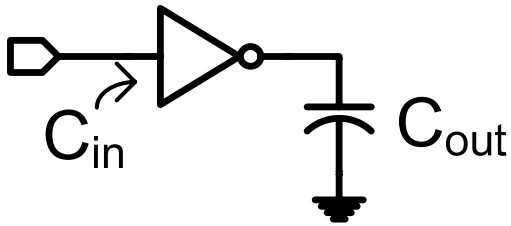
Logical Effort motivation

- Sizing of a chain of inverters
  - Geometric progression
- How about more complex logic?
- Logical Effort objectives:
  - Quick & dirty, back of the envelope sizing
  - Make trade-off between circuits
- Reference:
  - I. Sutherland, B. Sproull, D. Harris, *Logic Effort - designing fast CMOS Circuits* Academic Press, 1999

Delay : Output / Input load

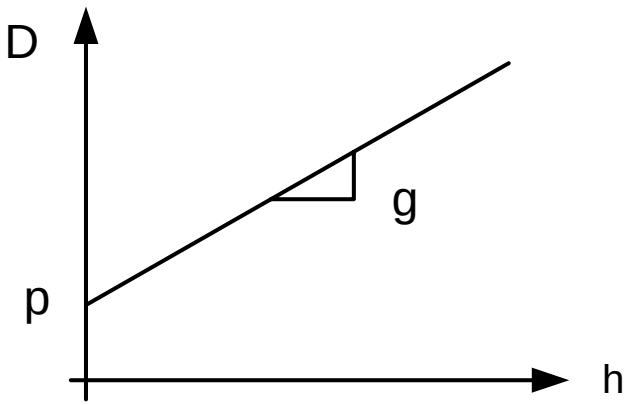
Let's model the delay as a function of the output / input load

$$D \approx RC_{sl} + RC_{in}\frac{C_{out}}{C_{in}}$$



Define $$h = \frac{C_{out}}{C_{in}}$$

$$D \approx \underbrace{R\,C_{sl}}_{p} + \underbrace{RC_{in}}_{g} \cdot h$$



$$D \approx p + g \cdot h \qquad f = g \cdot h$$

p = Parasitic (intrinsic) delay
g = Logical effort
h = Electrical effort
f = Effort delay or Stage effort

Figure of Merit

- Assume that rise delay = fall delay
  - Simplifying assumption, of reducing relevance
  - Therefore $R_p(inv) = R_n(inv)$
- Consider the RC product of a minimum sized gate.
  - $R_0 = R_p = R_n$
  - $C_0 = C_{in}$ (total input capacitance)
- As W varies as kW_{min},
  - RC product = $1/kR_0 * kC_0 = R_0C_0$

Figure of Merit - Inverter

- Consider an inverter with equal rise and fall delay.
  - Remember that size does not matter for figure of merit
  - For the sake of simplicity, consider a minimum sized inverter, $W_p = 2W_n = W_{min}$
    - $C_{in} = C_n + C_p = C_{min} + 2C_{min} = 3C_{min}$
    - $R_{eff} = R_{min}$
    - $\tau = R_{min} C_{min}$
    - RC product (in units of τ) = 3
- Evaluate all RC products in the same units to get delay
- In addition, by using a figure of merit which is relative to the inverter RC product, we get delay in units of inverter delay.

Units of effort

- Reference is the inverter:

$$g_{inv} = 1$$

$$p_{inv} = 0.6$$

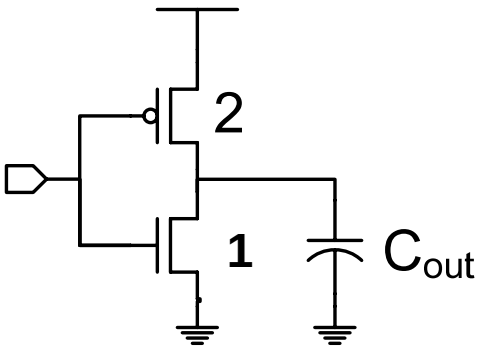
- g is a function of the complexity of a gate, not its size
  - Additional delay from driving its own input loading

- p is a function of the technology
  - Unloaded delay of a gate

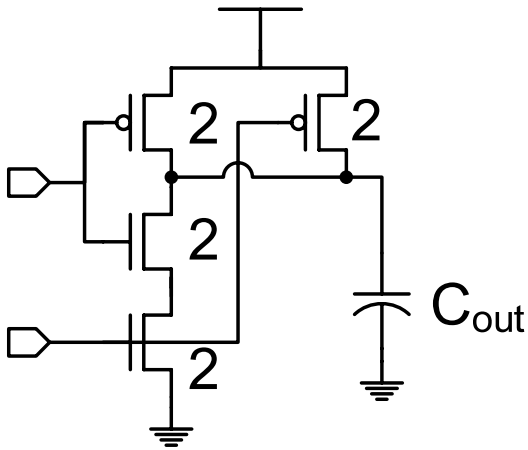
Logical effort

- Logic effort can be thought of the size of a gate relative to an inverter to produce the same output current as an inverter with the same output load

1. Inverter



2. 2-input NAND



$$f_1 = f_2$$

$$g_1 h_1 = g_2 h_2$$

$$1\frac{C_{out}}{3C} = g_2 \frac{C_{out}}{4C}$$

$$g_2 = \frac{4}{3}$$

$$C_{sd,inv} = 3C$$

$$C_{sd,nand} = 6C$$

$$p_2 = 2p_{inv}$$

Logical effort (g)

	Number of inputs					
Gate type	**1**	**2**	**3**	**4**	**5**	**n**
Inverter	1					
NAND		4/3	5/3	6/3	7/3	(n + 2)/3
NOR		5/3	7/3	9/3	11/3	(2n + 1)/3
Multiplexer		2	2	2	2	2
XOR (parity)		4	12	32		

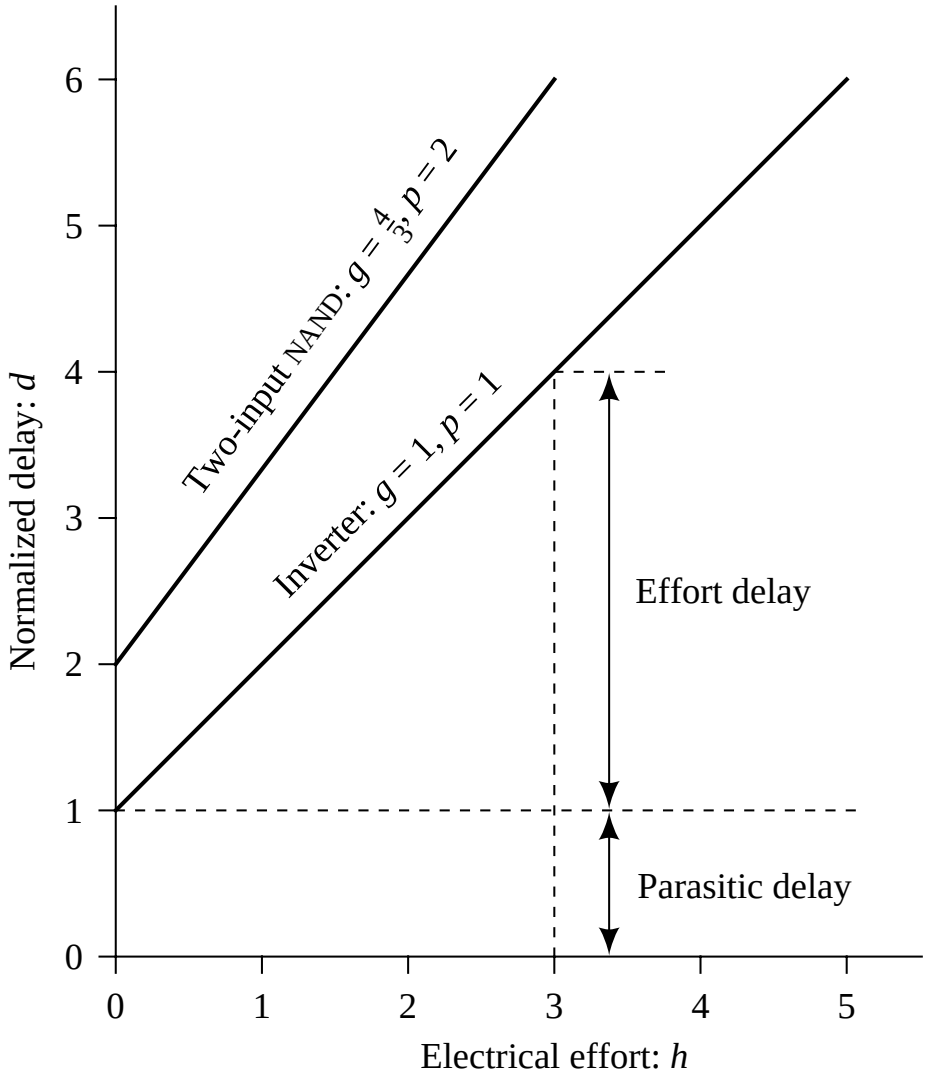
I. Sutherland, *et al*, Logical Effort, Academic Press, 1999

Parasitic Delay (p)

Gate type	Parasitic Delay
Inverter	p_{inv}
n-input NAND	$n.p_{inv}$
n-input NOR	$n.p_{inv}$
n-way multiplexer	$2n.p_{inv}$
XOR, XNOR	$4.p_{inv}$

I. Sutherland, *et al*, Logical Effort, Academic Press, 1999

Delay components



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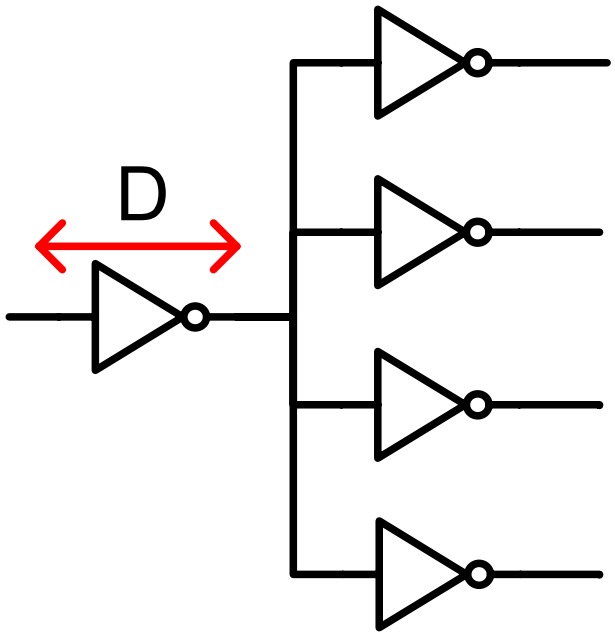
F04 Example



$$C_{out} = 4C_{in}$$

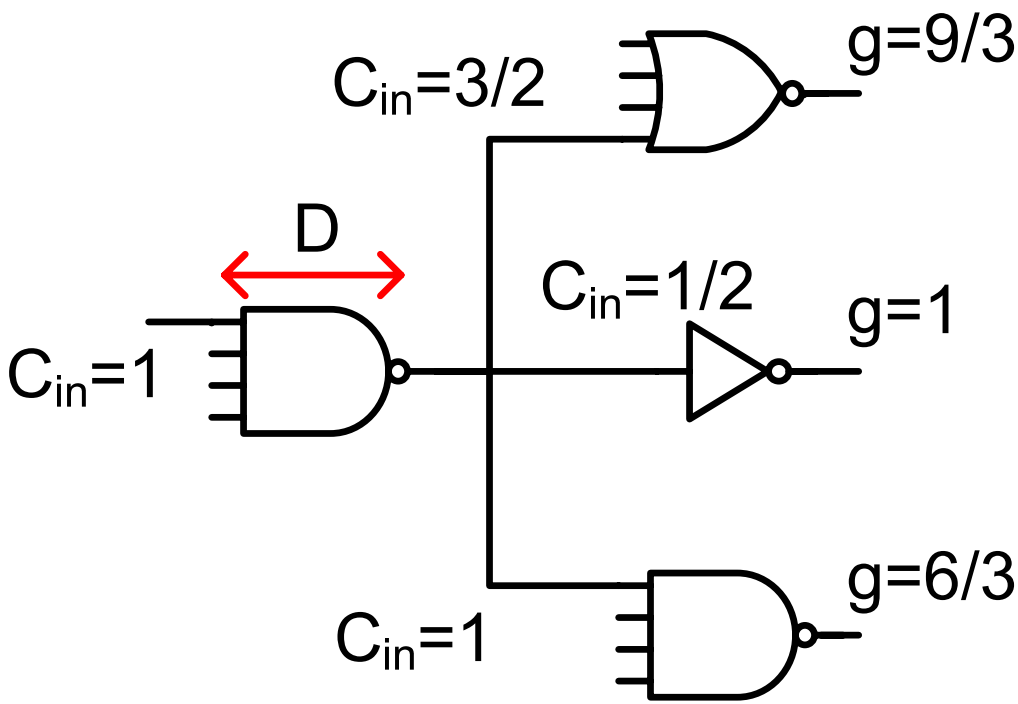
$$h = 4$$

$$g = 1$$

$$p = 0.6$$

$$D = 4 + 0.6 = 4.6\tau$$

More complex circuit



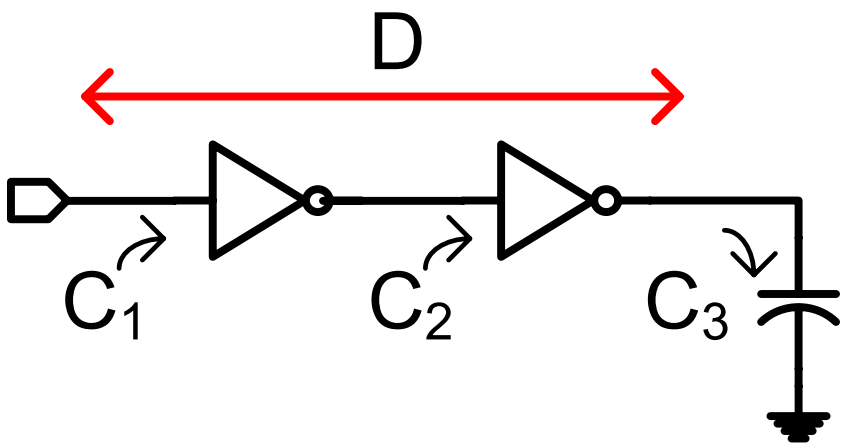
$$h = 3$$

$$g = \frac{6}{3}$$

$$p = 4 \times 0.6$$

$$D = 8.4\tau$$

Multistage effort



Defining the path effort H as:

$$H = \frac{C_3}{C_1}$$

$$h_1 = \frac{C_2}{C_1}$$

$$h_2 = \frac{C_3}{C_2}$$

$$\Rightarrow \quad H = h_1 h_2$$

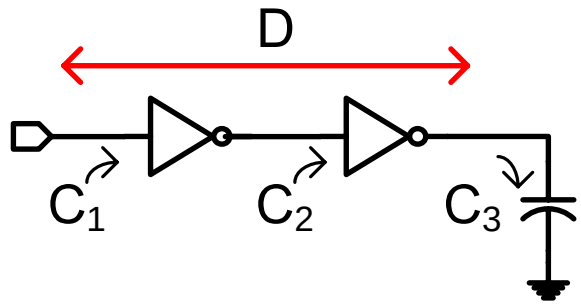
What was that homework problem all about??

- Recap of Question : Minimize the perimeter of a rectangle with dimensions w,h, for a constant area.
- Result is clearly a square.
- Corollary of a specific optimization problem which minimizes the sum of variables given the constraint that the product is constant

Minimum delay

D_1 D_2

Total delay $$D = g_1 h_1 + p_1 + g_2 h_2 + p_2$$



Substitute H $$D = g_1 h_1 + p_1 + g_2 \frac{H}{h_1} + p_2$$

$$\min\{D\} \Rightarrow \frac{\partial D}{\partial h_1} = g_1 - g_2 \frac{H}{h_1^2} = 0$$

Minimize the delay

$$g_1 - g_2 \frac{h_2}{h_1} = 0$$

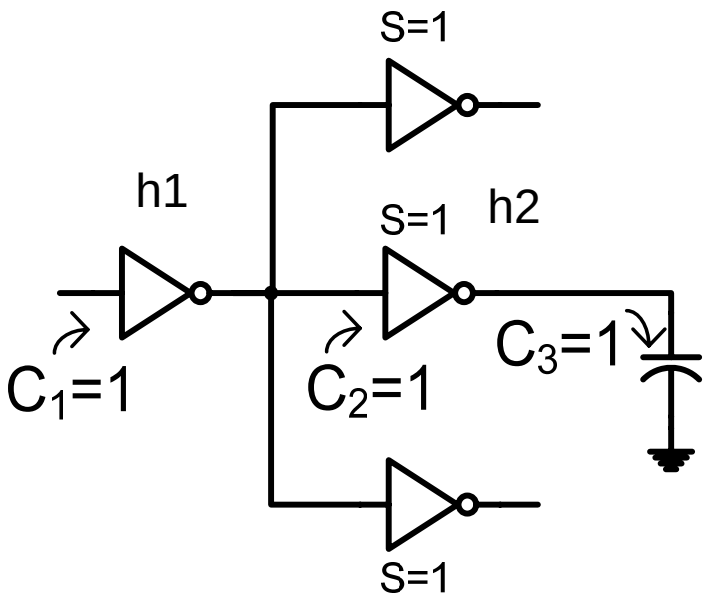
Solve for the minimum delay

$$g_1 h_1 = g_2 h_2$$

$$f_1 = f_2$$

Delay is optimal when the stage efforts are equal

Branching



Without branching: $H = h_1 h_2$

With branching: $h_2 = \frac{C_3}{C_2}$

$$h_1 = \frac{3C_2}{C_1}$$

$$h_1 h_2 = 3H$$

$$b_i = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$$

$$C_{on-path,2} = C_2$$

$$C_{off-path,2} = 2C_2$$

$$b_2 = \frac{3C_2}{C_2} = 3$$

Equivalent Path Efforts

$$H = \frac{C_{out}}{C_{in}}$$

$$B = \prod b_i$$

$$\prod h_i = BH$$

$$G = \prod g_i$$

Path Effort

$$F = GBH = \prod g_i h_i$$

Path Effort:

- Does not change with added inverters
- Does not depend on sizes, but on topology

Minimum Delay

$$F = GBH = \prod g_i h_i$$

Stage effort of stage i: f_i

$$g_i h_i = f_i$$

Optimal stage effort is:

$$\hat{f} = f_i$$

For N stages:

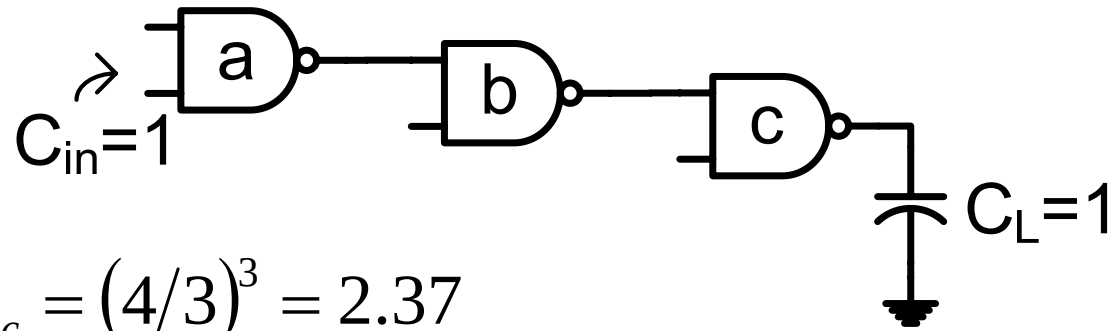
$$F = \hat{f}^N \Rightarrow \boxed{\hat{f} = F^{1/N}}$$

Minimum Delay:

$$\hat{D} = \sum_i g_i h_i + p_i$$

$$\hat{D} = N\hat{f} + \sum_i p_i = \boxed{N\hat{f} + P}$$

Example: compute min. delay



$$G = g_a g_b g_c = (4/3)^3 = 2.37$$

$$B = 1$$

$$H = C_L / C_{in} = 1$$

$$F = GBH = 2.37$$

$$\hat{f} = F^{1/3} = 4/3$$

$$\hat{D} = 3(2.37)^{1/3} + 3(2p_{inv})$$

$$\hat{D} = 4 + 6 \times 0.6 = 7.6\tau$$

Summary

- Instruction set and general 2-stage pipeline structure of the baseline processor
  - More on this in upcoming discussions
- Logic Effort:
  - Delay of an individual gate
  - Path delay
  - Minimum path delay