EECS 427
Lecture 7: Logic Effort – Continues…

Reading: handouts

Last Time

- Project overview
- Logic effort
  - Delay computation for individual gates
  - Comparison of gate topologies
- CAD 3 due on Monday Oct 2
- All teams finalized?
- Find project topic…
- HW1 graded

Outline

- Motivation
- Model the delay of one gate
- The delay of a chain of gates
- Branching
- Minimum delay
- Best number of stages and gate sizing
- Examples
- Limitations

Last time

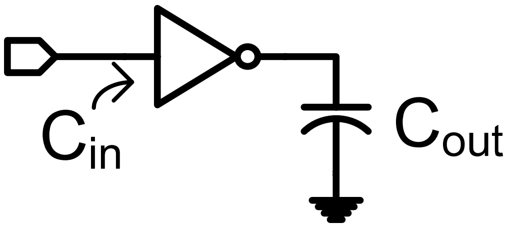
Review: Output / Input load

Let's model the delay as a function of the output / input load

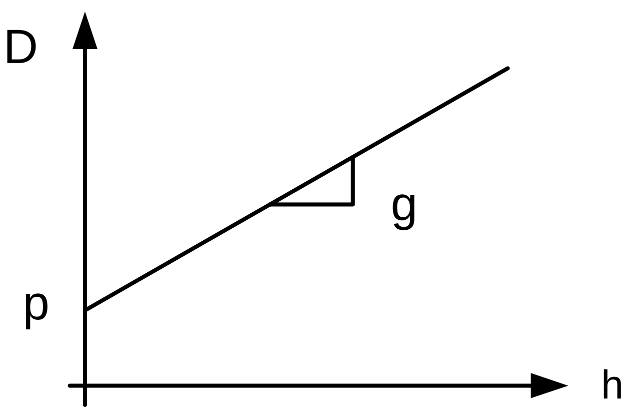
$$C_{in} = k_3 S$$

$$D \approx k_1 k_2 + k_1 k_3 \frac{C_{out}}{C_{in}}$$

Define $$h = \frac{C_{out}}{C_{in}}$$



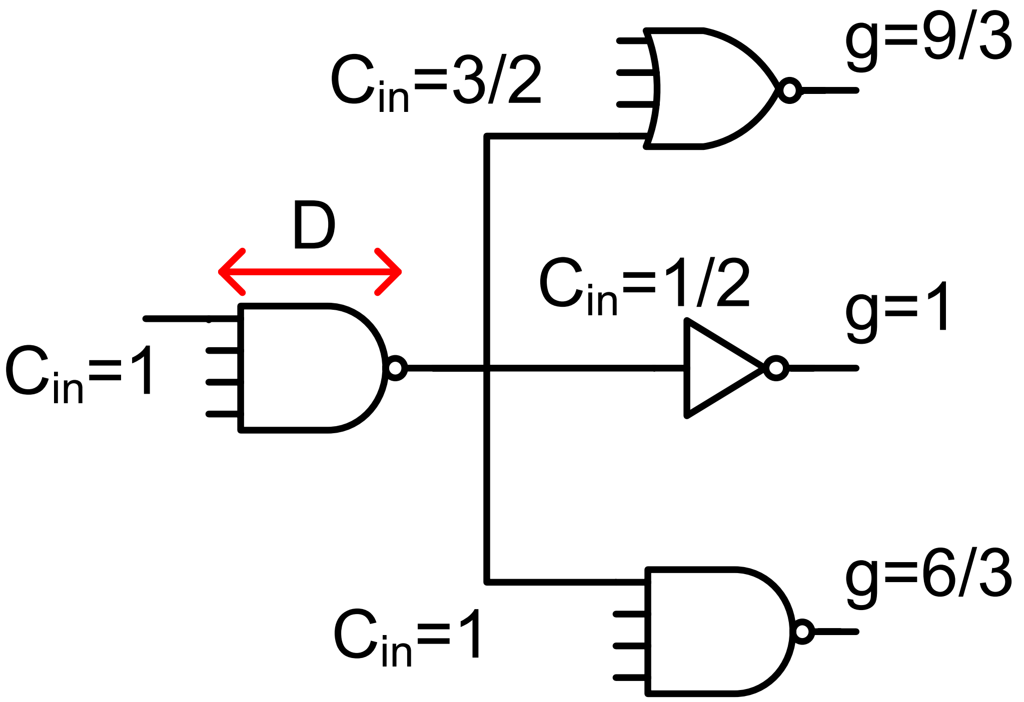
$$D \approx \underbrace{k_1 k_2}_{p} + \underbrace{k_1 k_3}_{g} \cdot h$$



$$D \approx p + g \cdot h \qquad f = g \cdot h$$

p = Parasitic (intrinsic) delay
g = Logical effort
h = Electrical effort
f = Effort delay or Stage effort

Review: More complex circuit



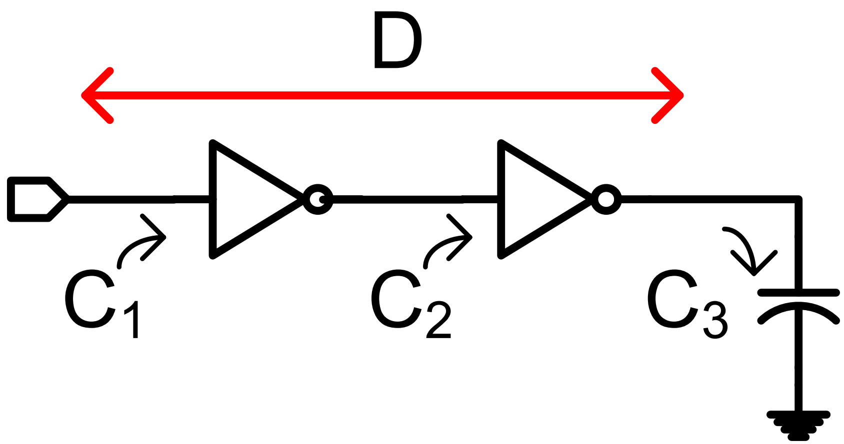
$$h = 3$$

$$g = \frac{6}{3}$$

$$p = 4 \times 0.6$$

$$D = 8.4\tau$$

Multistage effort



Defining the path effort H as:

$$H = \frac{C_3}{C_1}$$

$$h_1 = \frac{C_2}{C_1}$$

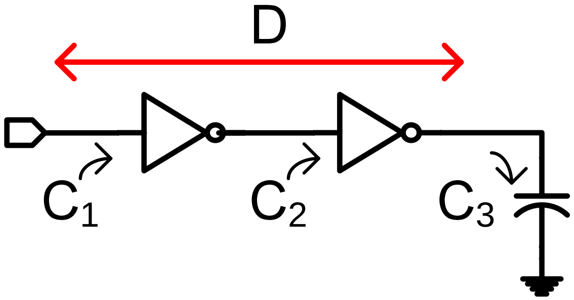
$$h_2 = \frac{C_3}{C_2}$$

$$\Rightarrow \quad H = h_1 h_2$$

Minimum delay

Total delay

$$D = \underbrace{g_1 h_1 + p_1}_{D_1} + \underbrace{g_2 h_2 + p_2}_{D_2}$$



Substitute H

$$D = g_1 h_1 + p_1 + g_2 \frac{H}{h_1} + p_2$$

$$\min\{D\} \Rightarrow \frac{\partial D}{\partial h_1} = g_1 - g_2 \frac{H}{h_1^{\,2}} = 0$$

Minimize the delay

$$g_1 - g_2 \frac{h_2}{h_1} = 0$$

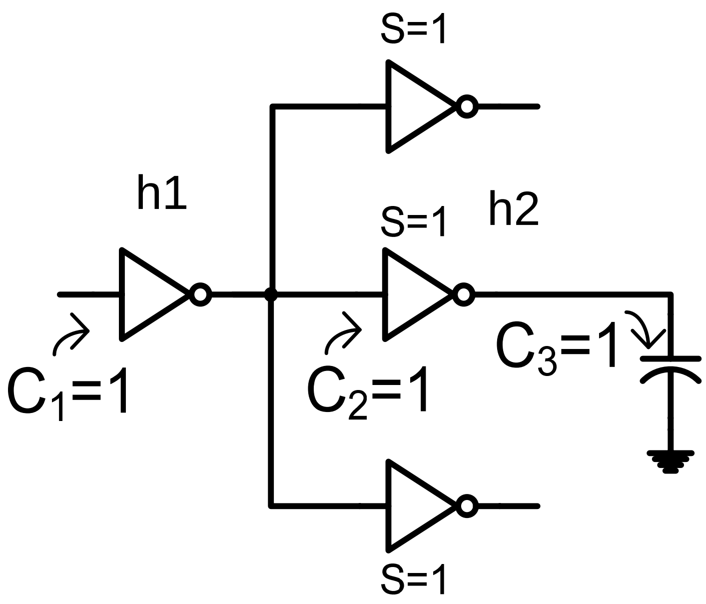
Solve for the minimum delay

$$g_1 h_1 = g_2 h_2$$

$$f_1 = f_2$$

Delay is optimal when the stage efforts are equal

Branching



Without branching: $H = h_1 h_2$

With branching: $h_2 = \dfrac{C_3}{C_2}$

$$h_1 = \frac{3C_2}{C_1}$$

$$h_1 h_2 = 3H$$

$$b_i = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$$

$$C_{on-path,2} = C_2$$

$$C_{off-path,2} = 2C_2$$

$$b_2 = \frac{3C_2}{C_2} = 3$$

Equivalent Path Efforts

$$H = \frac{C_{out}}{C_{in}}$$

$$B = \prod b_i$$

$$\prod h_i = BH$$

$$G = \prod g_i$$

Path Effort

$$F = GBH = \prod g_i h_i$$

Path Effort:

- Does not change with added inverters
- Does not depend on sizes, but on topology

Minimum Delay

$$F = GBH = \prod g_i h_i$$

Stage effort of stage i: f_i

$$g_i h_i = f_i$$

Optimal stage effort is:

$$\hat{f} = f_i$$

For N stages:

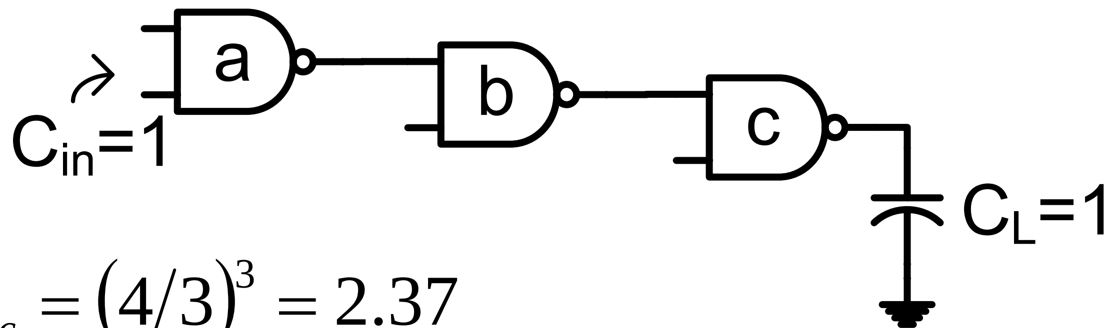
$$F = \hat{f}^{\,N} \Rightarrow \boxed{\hat{f} = F^{1/N}}$$

Minimum Delay:

$$\hat{D} = \sum_i g_i h_i + p_i$$

$$\hat{D} = N\hat{f} + \sum_i p_i = \boxed{N\hat{f} + P}$$

Example: compute min. delay



$$G = g_a g_b g_c = (4/3)^3 = 2.37$$

$$B = 1$$

$$H = C_L / C_{in} = 1$$

$$F = GBH = 2.37$$

$$\hat{f} = F^{1/3} = 4/3$$

$$\hat{D} = 3(2.37)^{1/3} + 3(2\,p_{inv})$$

$$\hat{D} = 4 + 6 \times 0.6 = 7.6\tau$$

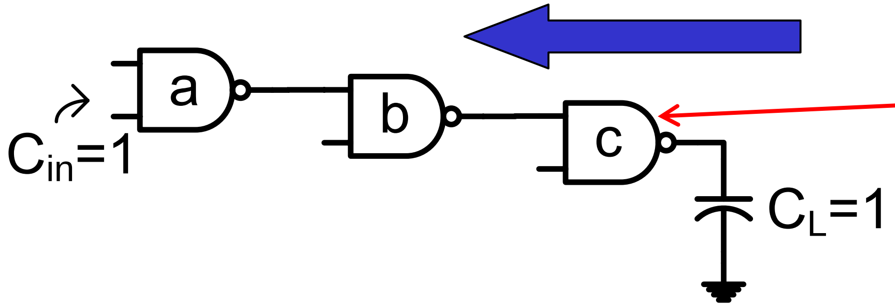
Stage sizing

After computing $\hat{f}$

$$h_i = \hat{f}/g_i = C_{out}/C_{in}$$

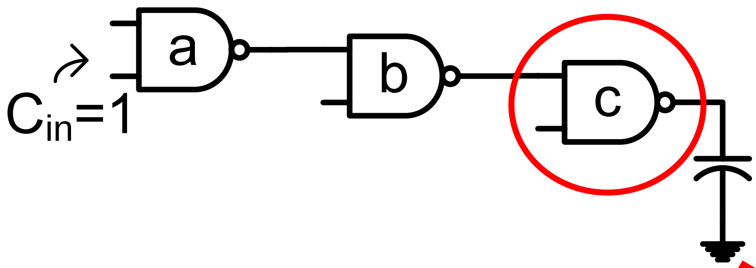
$$\boxed{C_{in} = \frac{g_i C_{out}}{\hat{f}}}$$

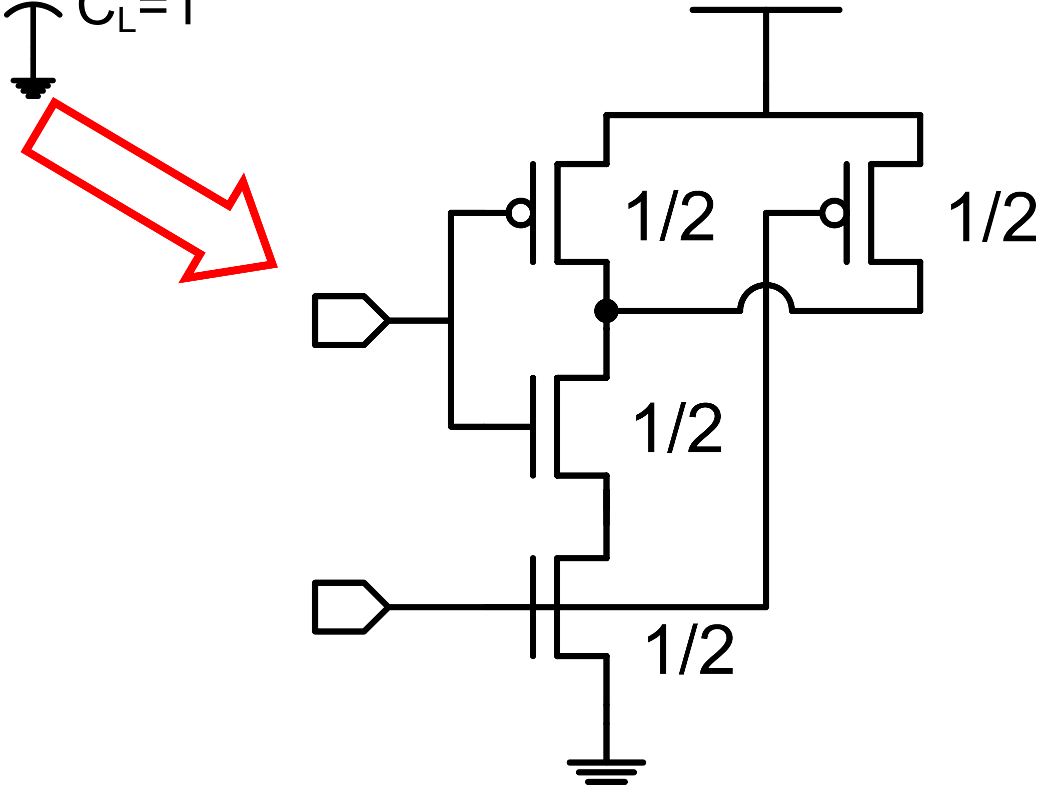
Work backwards to size each gate



$$C_{in,c} = \frac{g_{nand} C_{out}}{\hat{f}}$$

Stage sizing example





$$C_{in,c} = \frac{g_{nand} C_{out}}{\hat{f}}$$

$$C_{in,c} = \frac{4/3\,C}{4/3} = C$$

$$C_{in,c} = 4k \rightarrow k = \frac{1}{4}$$

Number of stages

- Path effort F can be used to determine the optimal number of stages
  - Assuming we add n_2 inverters
    - New number of stages $N=n_1+n_2$
    - G, B, H don't change - F is fixed
    - But P increases

$$\boxed{\hat{D} = NF^{1/N} + \sum_{i}^{n_1} p_i + (N - n_1)\, p_{inv}}$$

Optimum is technology dependent

Optimal stage effort

$$D = NF^{1/N} + \sum_{i}^{n_1} p_i + (N - n_1) p_{inv}$$

Assuming for now that N is differentiable

$$\frac{\partial D}{\partial N} = p_{inv} + F^{1/N}(1 - \ln F^{1/N})$$

Let ρ be the optimal stage delay. Then ρ satisfies:

$$\rho(1 - \ln \rho) + p_{inv} = 0$$

Best number of stages for $p_{inv} = 1.0\tau$

Path effort F	Best number of stages $\hat{f}$	Min. delay $\hat{D}$	Stage effort f
0		1.0	
	1		0-5.8
5.83		6.8	
	2		2.4-2.7
22.3		11.4	
	3		2.8-4.4
82.2		16.0	
	4		3.0-4.2
300		20.7	
	5		3.1-4.1
1090		25.3	
	6		3.2-4.0
3920		29.8	
	7		3.3-3.9
14200		34.4	

I. Sutherland, *et al*, Logical Effort, Academic Press, 1999

Summary of the method

Gate level		**Path**	
Parasitic delay	p	Path electrical effort	$H = \frac{C_{out-path}}{C_{in-path}}$
Logical effort	g	Path logical effort	$G = \prod g_i$
Electrical effort	$h = \frac{C_{out}}{C_{in}}$	Branch effort	$B = \prod b_i$
			$\prod h_i = BH$
Stage effort	$f = gh$		
Stage delay	$d = f + p$	Branching factor	$b_i = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$

Method

Path effort $F = GBH$

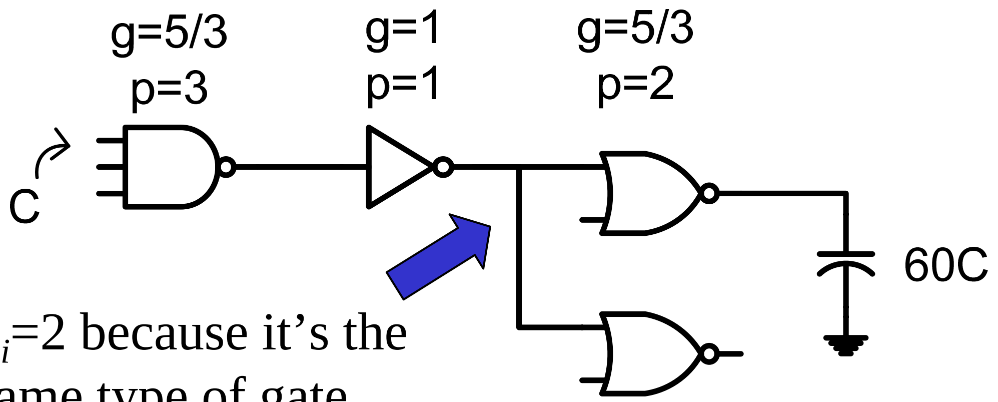
Optimal stage effort $\hat{f} = F^{1/N}$

Optimal path delay $\hat{D} = NF^{1/N} + P$

Stage sizing $C_{in} = \dfrac{g_i C_{out-stage}}{\hat{f}}$

1. Compute path effort
2. Add buffers (determine optimal number of stages)
3. Compute optimal stage effort and minimum delay
4. Size individual gates (working backwards)

Method example 1/3



b_i=2 because it's the same type of gate

$$G = \frac{5}{3} \cdot 1 \cdot \frac{5}{3} = \frac{25}{9}$$

$$B = 1 \cdot 2 \cdot 1 = 2$$

$$H = 60$$

$$\sum p_i = 3 + 1 + 2 = 6$$

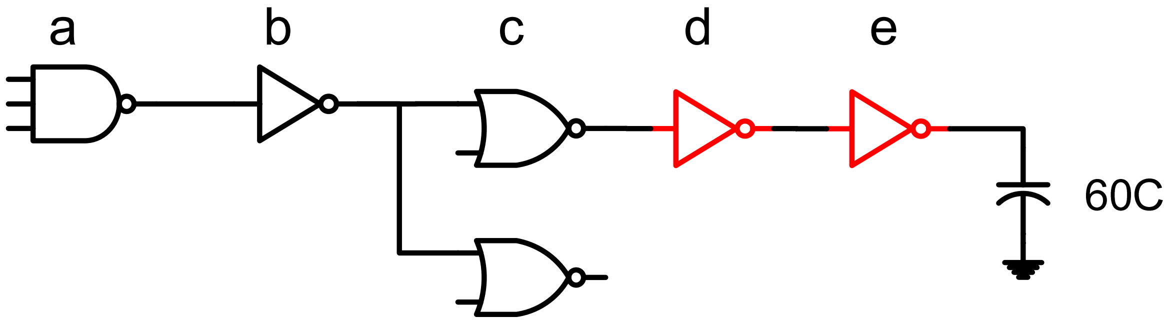
$$F = GBH = 333.33 \rightarrow \hat{N} = 5$$

$$\hat{D} = 5(333.33)^{1/5} + 6 + 2 = 24\tau$$

$$\hat{f} = (333.33)^{1/5} = 3.2$$

- From the table, the optimum number of stages for F=333.33 is 5.
- We have to add 2 inverters to the existing 3 stages.

Method example: Sizing 2/3



$$C_{in,e} = \frac{g_i C_{out,e}}{\hat{f}} = \frac{1 \times 60C}{3.2} = 18.75C$$

$$C_{in,d} = \frac{1 \times 18.75C}{3.2} = 5.86C$$

When there is a branch:

$$C_{in} = \frac{g_i C_{out} b_i}{\hat{f}}$$

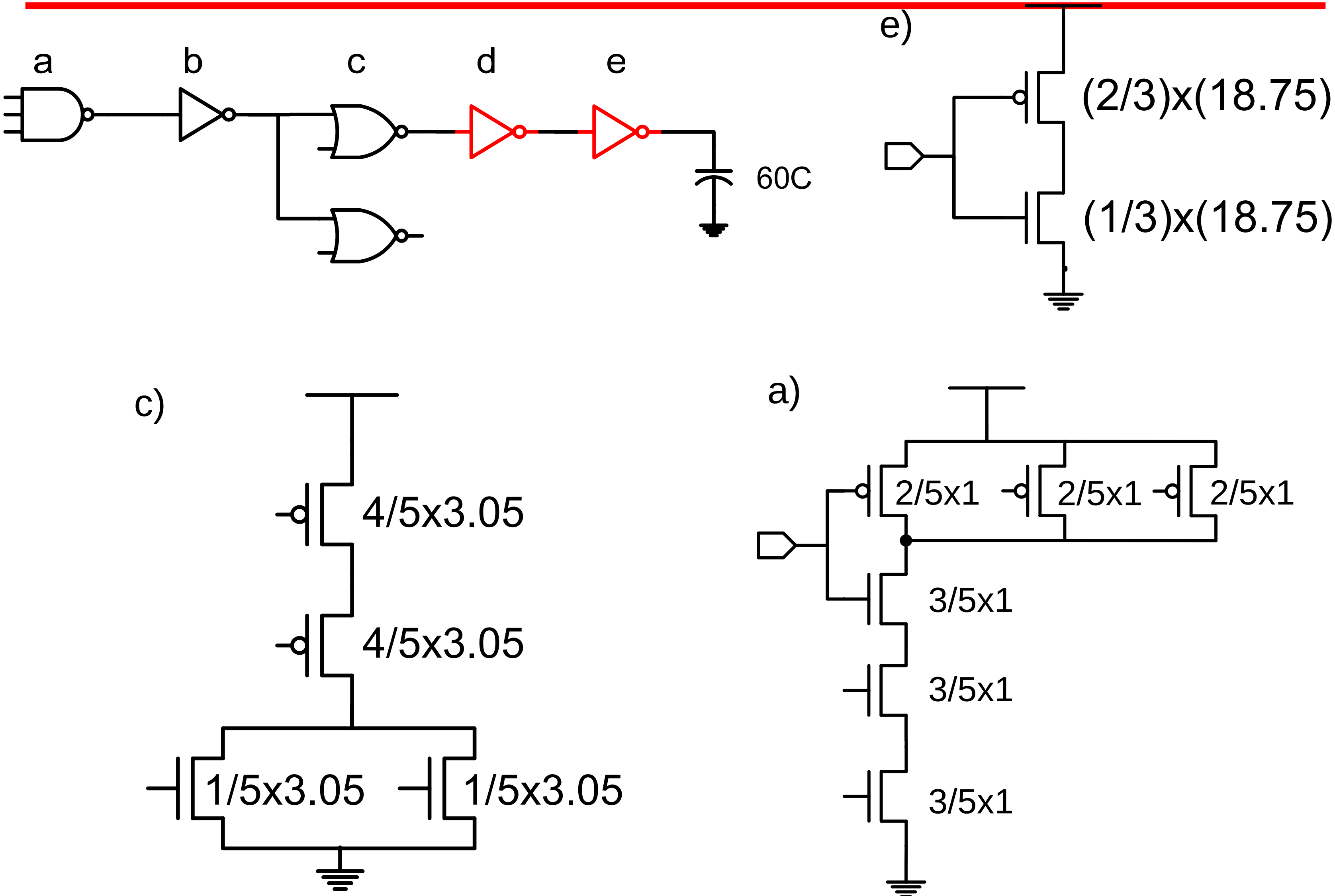
$$C_{in,c} = \frac{5/3 \times 5.86C}{3.2} = 3.05C$$

$$C_{in,b} = \frac{1 \times 3.05C \times 2}{3.2} = 1.96C$$

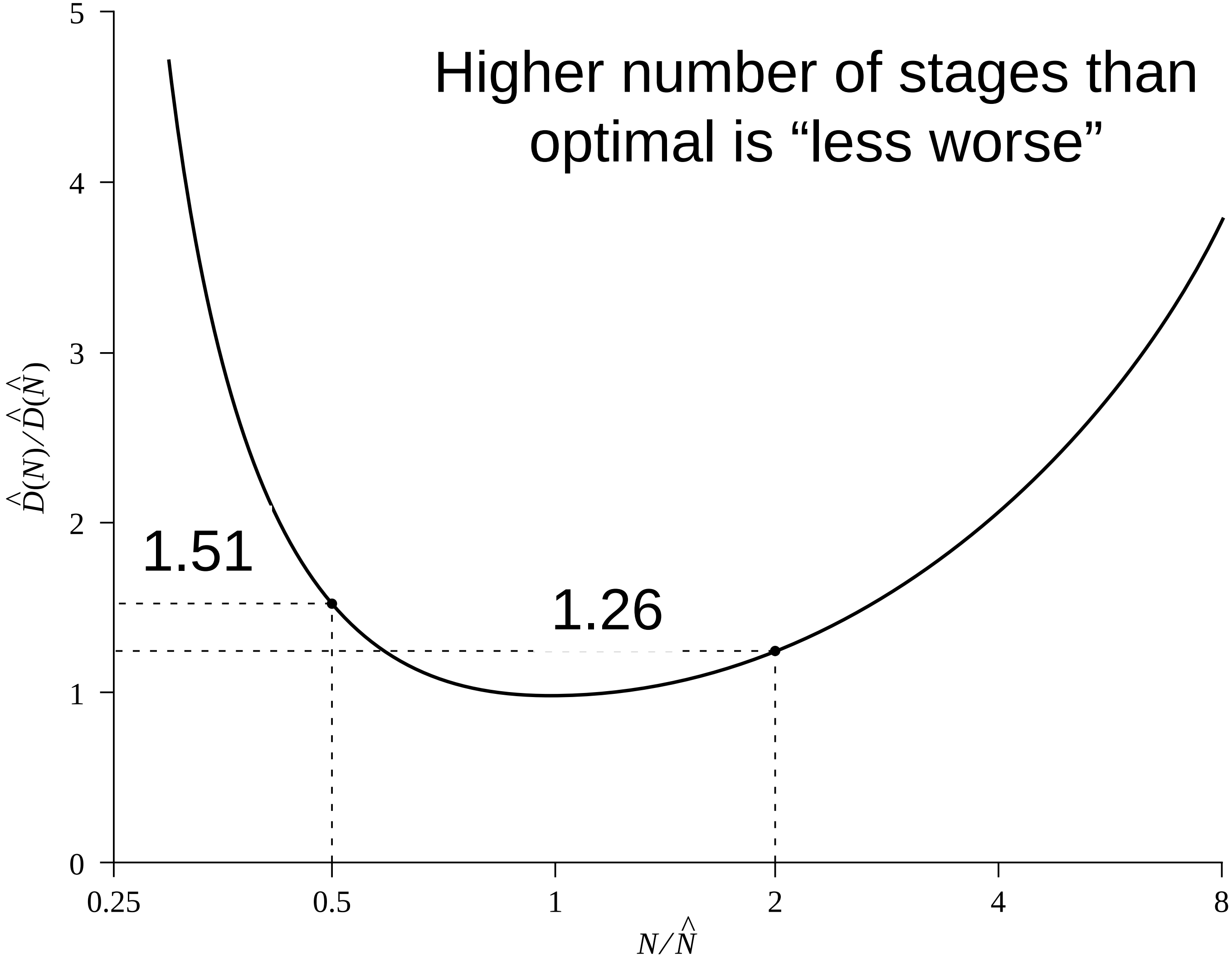
$$C_{in,a} = \frac{5/3 \times 1.9C}{3.2} = 0.989C \approx C$$

Always check this

Method example: sizing 3/3

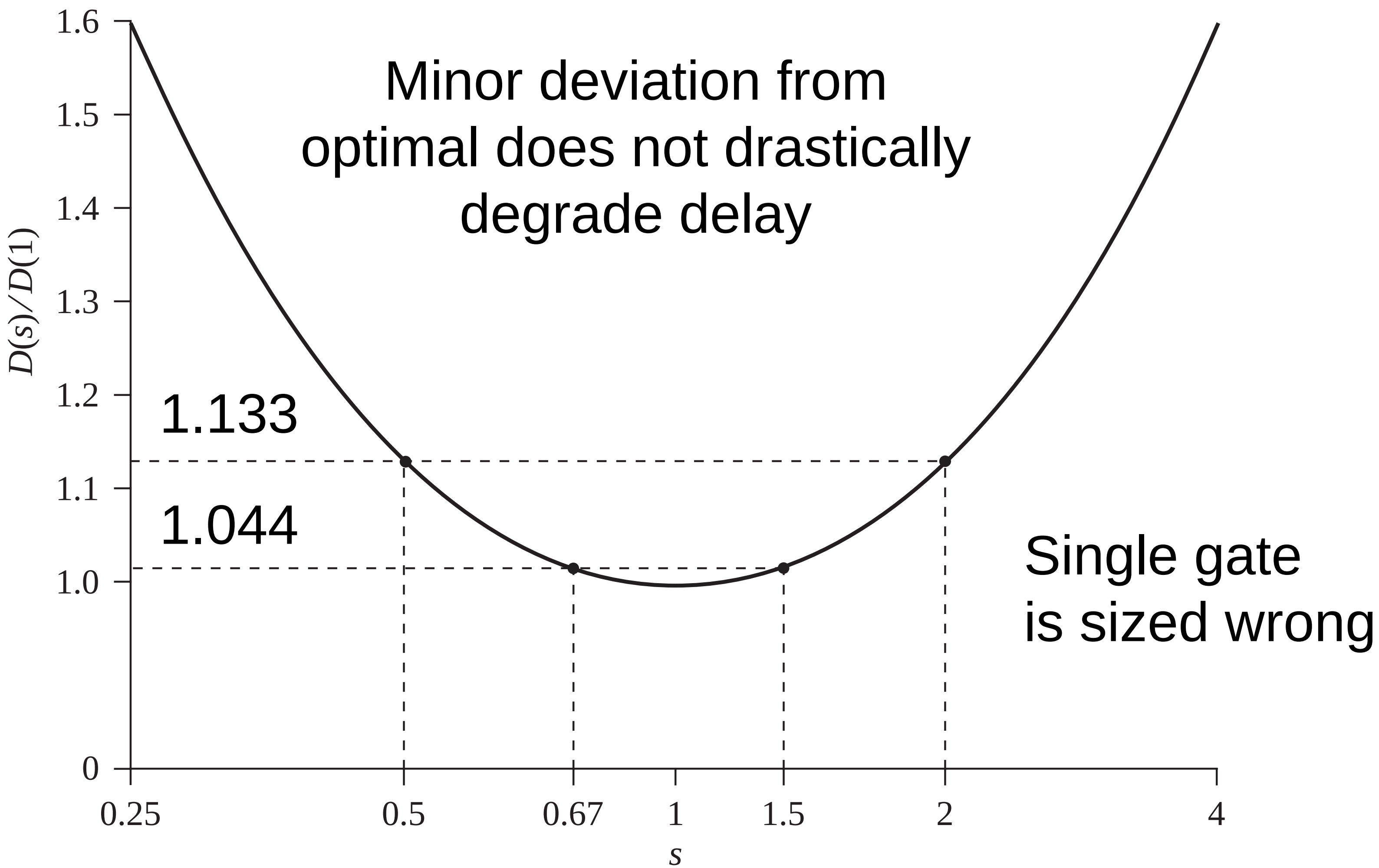


Wrong number of stages



I. Sutherland, *et al*, Logical Effort, Academic Press, 1999

Wrong gate size



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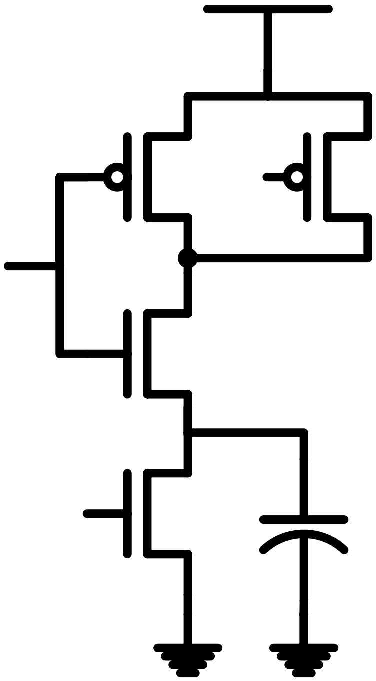
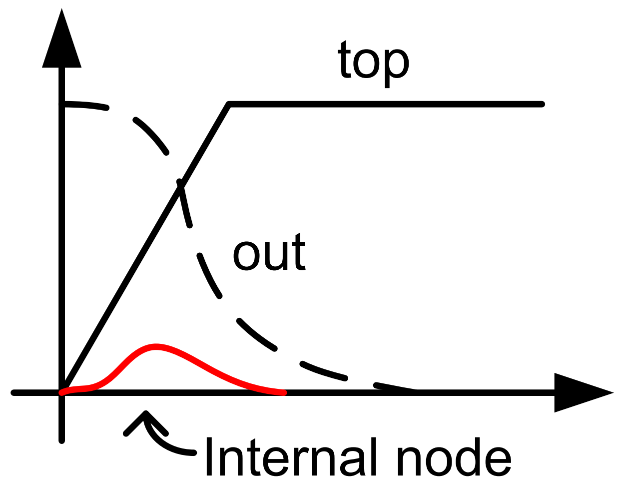
Limitations – Internal capacitance

- Capacitance in internal nodes
- Body effect

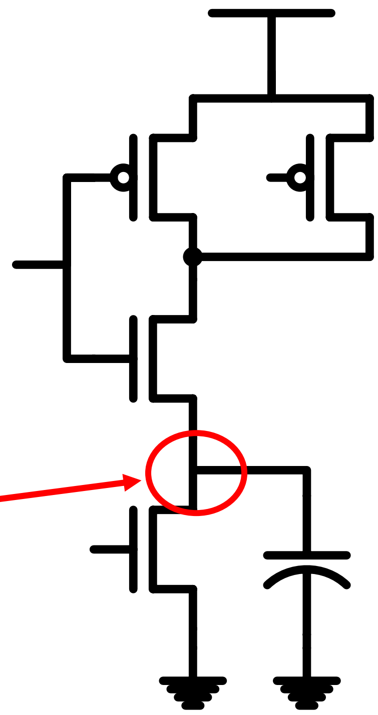




Limitations - Tapering

- Optimal transistor sizes in stack are different (latest input at top of stack)
- What size is the best choice?

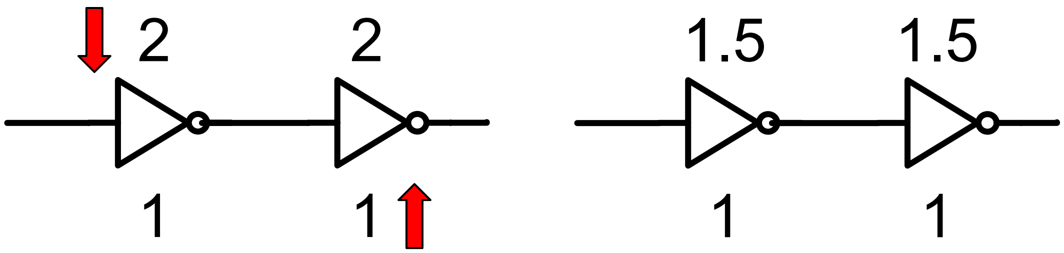
Same cap in internal node



5	4	6
5	6	4

Limitations – P/N ratio

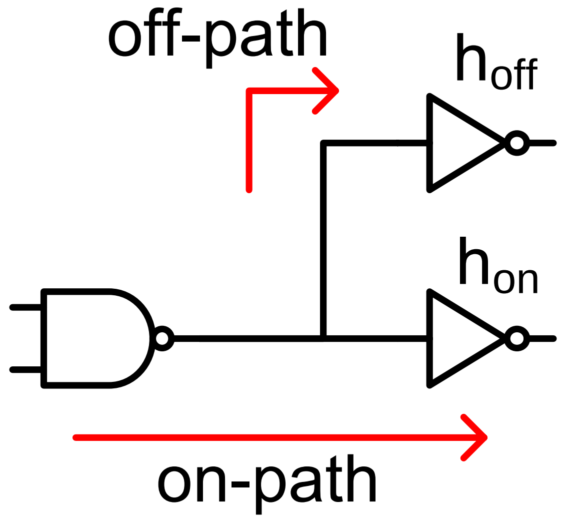
- Why use P/N = 2?
  - Noise margins are balanced
  - Equal slopes
- How about P/N = 1.5?



  - Decrease by 0.1 → Delay increased by 5%
  - Increase by 0.1 → Delay decreased by 10%

Limitations – Branching

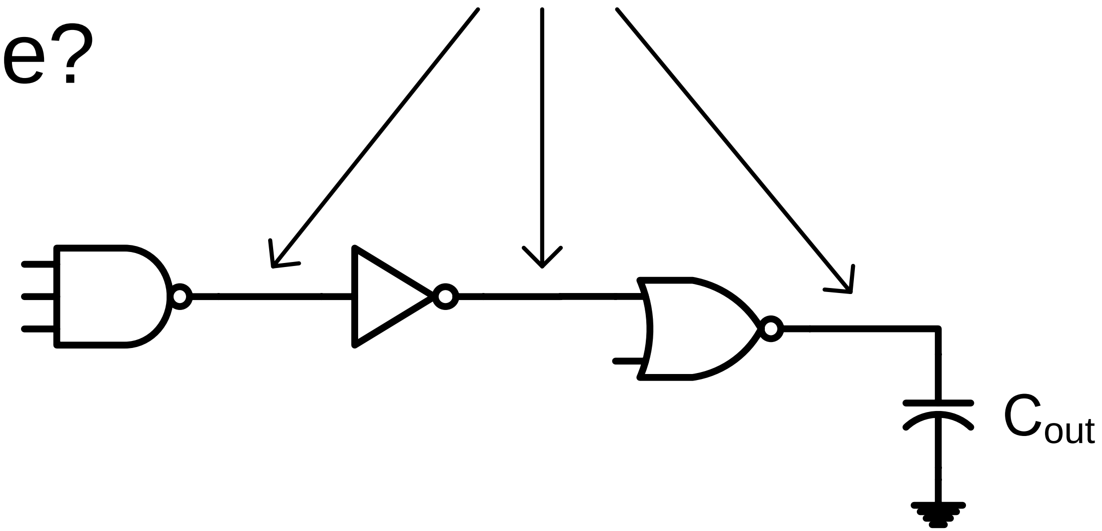
- Assume that the size of the off-path gate tracks the size of the gate on-path



- Sizing one “critical” path of a branch may make the other paths worse

Limitations - Slope

- Different slew rates
- Where is it best to insert additional size?



Limitations - Scaling

- Scaling is not linear with width

$$d \approx RC$$

$$C = k_c S \Rightarrow C = k_c S + k_p$$

Perimeter

but really

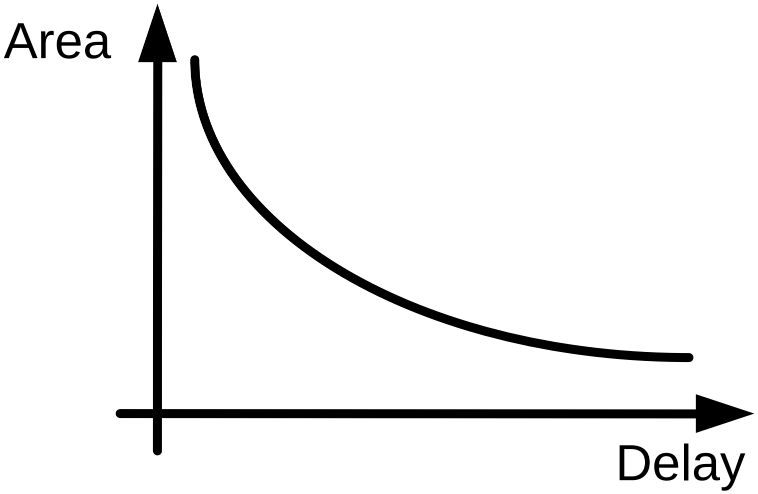
$$R = \frac{k_R}{S} \Rightarrow R = \frac{k_R}{S} + k_v$$

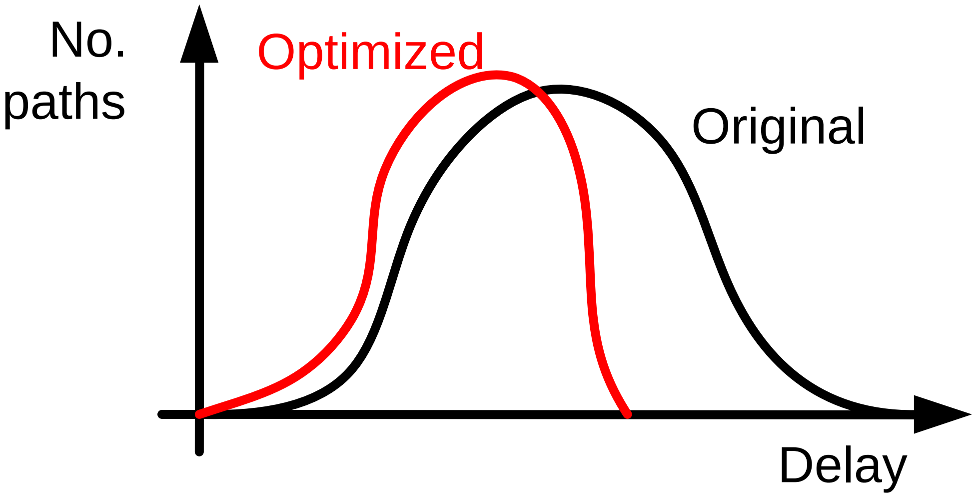
Narrow width effects
Process variations

Sizing tool

- Tool: TILOS [Dunlop 89]
  - Start with all transistors of min. size
  - Find critical path (Optimize path)
  - Compute delays
  - Increase size of “critical path”
  - Size transistor with best sensitivity in critical path
  - Repeat
  - Goal of path distribution → All paths equal in length…

Area - Delay





But the impact of process variations can be worse for the optimized paths

Summary

- Logic Effort
  - Compute path effort, stage effort, sizes
  - Sizing on the back of an envelope!
- Limitations of method
  - Only min delay sizing
  - Tapering and internal stack effects
  - Branching effort not realistic
    - Unnecessarily constraints “side” gates to scale their sizes along with gate on critical path
    - Particularly a problem when you think of wire capacitance as “branching” load.