University of Michigan
EECS 522: Analog Integrated Circuits
Winter 2009

CAD 1

Issued 2/6/2009 – Due 2/20/2009

CAD 1.1: Getting (re)acquainted with using Cadence and the IBM $0.13\mu m$ CMOS process for noise simulations.

a) We will use Cadence for schematic capture, simulation, and layout of all circuits in this class. Two tutorials, **Tutorial 1** and **Tutorial 2**, have been placed on the course website that walk through the configuration and basic use of Cadence and the IBM process. Work through both of these tutorials. For those of you who took 413, the setup is similar but review the first page of Tutorial 1 for the links and directories for 522.

b) Copy the RF examples library to your eecs522 working directory (created in Tutorial 1):
cp -rf /usr/caen/ic-5.141_usr4/tools/dfII/samples/artist/rfExamples ~/eecs522/CAD

c) Before opening Cadence, open the **cds.lib** file in your eecs522 directory and append the following lines:
DEFINE ahdlLibLib $CDS/tools/dfII/samples/artist/ahdlLib
DEFINE rfLib $CDS/tools/dfII/samples/artist/rfLib
DEFINE pllLib $CDS/tools/dfII/samples/artist/pllLib
DEFINE rfExamples ~/eecs522/CAD/rfExamples

d) The **Spectre RF Manual** has been placed on the course website. Familiarize yourself with **Chapter 6** of this document on simulating low noise amplifiers using S-parameters. The manual may also be found at the following link.
/usr/caen/ic-5.141_usr4/doc/spectreRF/spectreRF.pdf

CAD 1.2: In this problem you'll extract g_m, g_{d0}, and $\alpha = g_m/g_{d0}$ as a function of current density (I_D/W) for two devices.

a) Generate a schematic that will allow you to extract the transconductance (g_m) of an *nfet_rf* at a fixed V_{DS} of 0.5V and the 0V conductance (g_{d0}) of an *nfet_rf* while sweeping V_{GS} from 0 to 1.2V. Do this by placing two identical *nfet_rf*'s on one schematic, with the different V_{DS} biases applied, and performing a DC sweep of V_{GS}. Replicate this circuit on your schematic to allow you to extract g_m and g_{d0} for two different W/L ratios of $200\mu m/120nm$ and $200\mu m/180nm$.
Use the **nfet_rf** component in the **cmrf8sf** library, for this part leave the number of fingers equal to 1.

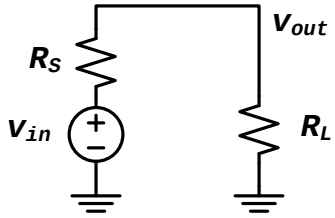
b) Use the parametric analysis tool (Analog Design Environment > Tools > Parametric Analysis…) to perform a sweep of V_{GS} from 0 to 1.2V, performing a DCop at each point. Setup an output in Analog

Environment to calculate and save the current *density* $I_{den} = I_{DS}/W$. Extract plots of I_{den}, g_m, g_{ds}, and α as functions of V_{GS}. It is not necessary to turn in these plots.
Hint: Within the calculator, you can use OP("/TN0","gm") and OP("/TN0","gds") to extract and plot g_m and g_{ds} of device *TN0*.

c) Using the parametric analysis from a) and saved I_{den} from b), generate one plot with g_m and g_{d0} vs. I_{den} for the $200\mu m/120nm$ device, and a second plot for the $200\mu m/180nm$ device. In Cadence you can plot vs. a saved output (I_{den}) by double-clicking the x-axis of a plot and selecting the output. Generate two additional plots of α vs. I_{den} for the two devices. Print out your plots and turn them in. Use the **File > Print** command in AE and select the **print to file** to generate an EPS file. Do not turn in screen captures.

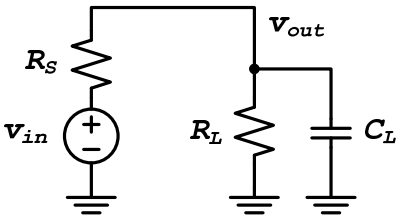
CAD 1.3: Simulating the noise spectral density and noise factor.

a) For the circuit on the right, calculate numerical values of output mean-square voltage spectral density ($\bar{v}_{out}^2/\Delta f$) and noise factor for $R_S = R_L = 50\Omega$.



b) Generate a schematic for the circuit shown on the right. Use an input port with impedance of 50Ω (this is R_S) and add a resistor $R_L = 50\Omega$. Simulate the noise spectral density ($\bar{v}_{out}^2/\mathrm{Hz}$) and the noise factor and compare these with your calculations in a).
Hint: You can use the **noise** analysis for this part.

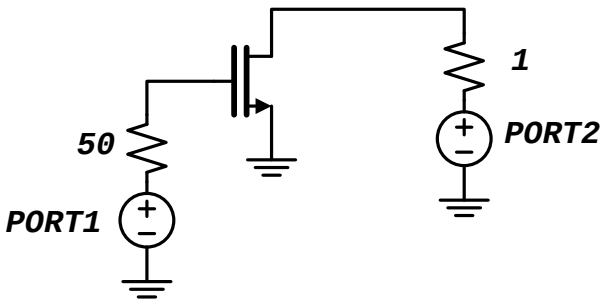
c) Now add a load capacitor C_L to the circuit as shown on the right. Calculate a numerical value for the total output RMS voltage with $C_L = 125pF$.



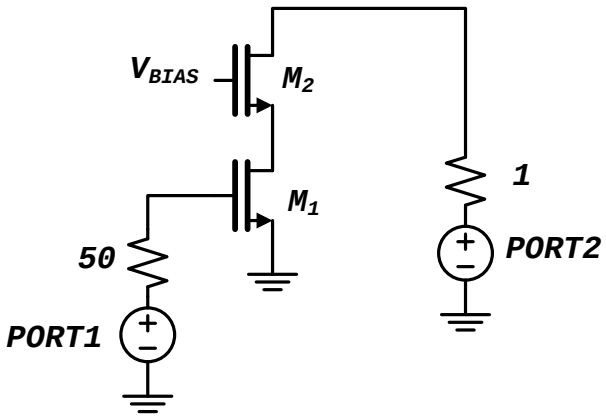
d) Simulate the noise spectral density at the output from 1kHz to 10GHz. Using the calculator, integrate the noise spectral density over this frequency range and find the RMS output noise voltage. Compare with your answer from part c).
Turn in a printout the noise spectral density.

CAD 1.4: Compare the noise figure of a CS amplifier with cascoding.

a) Simulate the noise figure of the circuit shown on the right using an *nfet_rf* with $W/L = 200\mu m/120nm$, $V_{GS} = 500mV$, and $V_{DS} = 500mV$. Turn in a plot of the NF and minimum NF from 1kHz to 10GHz.
Note: ports may be used for DC bias, however be aware that the DC voltage is doubled from the value entered in the form (assuming matched load).

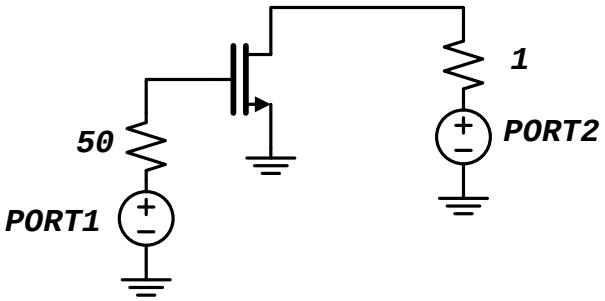


b) Next simulate the circuit shown on the right with a cascode device, the bias voltage $V_{BIAS} = 0.9V$, drain voltage on M_2 is $V_{D2} = 0.9V$, and the sizes of the *nfet_rf*'s are the same as in a). Turn in a plot of the NF and minimum NF from 1kHz to 10GHz.



c) What are the noise corner frequencies of the two circuits (intersection of 1/f noise and drain thermal noise).

CAD 1.5: Extracting FET parameters.



a) Perform a DC operating point simulation on the circuit shown to the right using an *nfet_rf*. Give the FET a $V_{GS} = 0.5V$ and $V_{DS} = 0.5V$. Bring up the Results Browser in Analog Environment (**Tools > Results Browser**). Choose **modelParameter-info**, and select the FET (e.g. "T0"), then **nch**. All model parameters appear on the right. Right-click on a variable (e.g. "ntnoi") and select "Table" to print the value with its corresponding units, or "Calculator" to generate a calculator expression to import the value into the calculator. Following the syntax, calculate C_{ox} as *cgsl / dlc* in the calculator and verify you get $0.01833\ F/m^2$. Find the value of μ_0 (variable u0). You can get V_{th} by choosing the **dcOpInfo-info** and selecting the FET, then the *vth* variable. Note *gm* and *gds* also appear here.

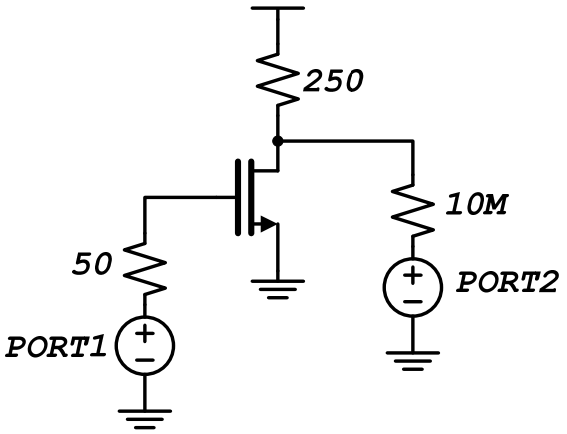
b) In this part you'll approximate the excess noise factor γ used in our drain thermal noise model in class.

$$\bar{i}_d^2 = 4kT\gamma g_{d0}\Delta f$$

We can approximate $\gamma = NTNOI$, where the BSIM4 variable *ntnoi* can be found in the Results Browser, and g_{d0} is the 0V conductance found in CAD 1.2. Using the Parametric Analysis tool for the circuit above, examine how *ntnoi* changes as a function of I_{den}. As before, sweep V_{GS} from 0 to 1.2V, with $V_{DS} = 500mV$, with W/L = $200\mu m/120nm$. Print and turn in this plot.

c) In this part you will examine how *ntnoi* (γ) changes as a function of gate length. Using the Parametric Analysis tool, setup a sweep of L from 120nm to 500nm with $W = 200\mu m$. Bias the FET with $V_{GS} = 500mV$ and $V_{DS} = 500mV$.

CAD 1.6: Noise of a common-source amplifier with resistive load. Use $V_{DD} = 1.2V$, $V_{GS} = 500mV$, $W/L = 200\mu m/120nm$. Use an *nfet_rf* device with the number of fingers equal to 1.



a) Derive equations for the input and output spectral densities ($\overline{v_i^2}/\Delta f$, $\overline{v_o^2}/\Delta f$) including thermal noise from the load resistor, thermal noise from the drain, and gate noise from gate resistance only (ignore flicker noise). Assume a gate resistance of $R_G = 3k\Omega$. Substitute the Cadence extracted values for NTNOI, gd0, gds, and gm, and calculate the value of the noise spectral densities.

b) Simulate the noise in the amplifier from 1kHz to 10GHz. Use Cadence to plot the input and output spectral densities ($\overline{v_i^2}/\Delta f$, $\overline{v_o^2}/\Delta f$). Compare your hand calculations with the simulation.

CAD 1.7: A FET with have thermal noise due to gate resistance. The thermal noise is modeled using the Thevenin model for a resistor with

$$\bar{v}_g^2 = 4kTR_g\Delta f, \qquad R_g \approx RSHG\frac{W}{L \cdot N_{finger}^2 \cdot N_{contact}^2}$$

where W and L are the total drawn width and length, N_{finger} is the number of fingers, $N_{contact}$ is the number of gate connections (use $N_{contact} = 2$), and $RSHG$ is the gate sheet resistance (Ohm/square). Extract $RSHG$ using the ResultsBrowser in Cadence.

a) For the circuit above, calculate how many fingers are required to make thermal noise from gate resistance equal to the input-referred short-circuit noise voltage from other noise sources in the circuit (neglecting input noise).

b) Simulate the input-referred mean-square noise voltage for the circuit with N_{finger} of 1, 20, and the value chosen in a). Comment on the results, how does the noise improve beyond the calculated number of fingers?