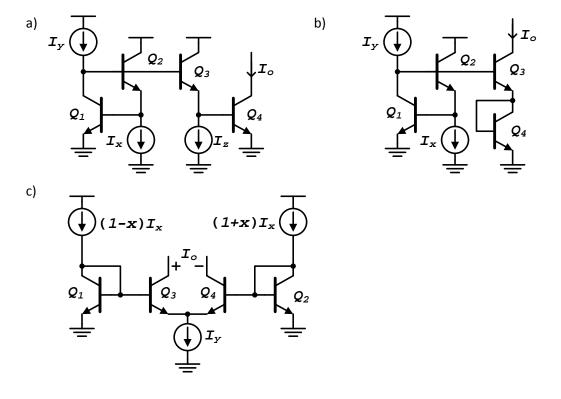
## University of Michigan EECS 522: Analog Integrated Circuits Winter 2009

## Problem Set 4

## Issued 3/4/2009 - Due 3/11/2009

**Problem 4.1:** Find expressions relating the large-signal output current I<sub>o</sub> to the other current sources in the circuits below. You may ignore base current. You may also find the following reference useful: B. Gilbert, "Translinear circuits: a proposed classification," *Electronics Letters*, Vol. 11, No. 1, Jan. 1975, pp. 14-16.



**Problem 4.2:** For this problem, assume an amplifier with harmonic distortion terms up to 3<sup>rd</sup> order, and all higher order terms may be neglected:  $v_{out} = \alpha_1 v_{in} + \alpha_2 v_{in}^2 + \alpha_3 v_{in}^3$ . The gain of the amplifier is 10dB, and HD<sub>3</sub> is -40dB, measured at an input level of -15dBm in a 50 $\Omega$  environment.

- a) Estimate IM<sub>3</sub> of the amplifier at an input power level of -15dBm.
- b) Assuming the input power was measured in a  $50\Omega$  environment; find the values of  $\alpha_1$  and  $\alpha_3$  for the amplifier.
- c) Sketch a generic plot of the 3<sup>rd</sup>-order intercept point. Calculate the values of IIP3 and OIP3.

**Problem 4.3:** For this problem, assume an amplifier with harmonic distortion terms up to  $3^{rd}$  order, and all higher order terms may be neglected:  $v_{out} = \alpha_1 v_{in} + \alpha_2 v_{in}^2 + \alpha_3 v_{in}^3$ . The gain of the amplifier is 10dB, and HD<sub>2</sub> is -20dB, measured at an input level of -20dBm in a  $50\Omega$  environment.

- a) Calculate the DC offset in Volts at the output due to the 2<sup>nd</sup>-order harmonic distortion in the amplifier at an input level of -20dBm.
- b) What input level in dBm is required to reduce the DC offset at the output to 1mV.

**Problem 4.4:** You are given that an amplifier has a measured HD2, HD3, and HD4 of -30dB, -40dB, and -50dB, respectively. Assuming there are no other significant harmonics, calculate the THD in percent.

**Problem 4.5:** Use the circuit on the right for this problem. Consider only thermal noise in  $R_S$ , drain thermal noise in the FET, and correlated gate noise in the FET. You may neglect body effect and channel length modulation. Include  $C_{GS}$ , but ignore all other caps.

- a) Find expressions for the input referred short-circuit noise voltage and open-circuit noise current of the amplifier (not including  $Y_S$ ).
- b) Find expressions for  $B_{S,opt}$  and  $G_{S,opt}$  ( $Y_S = G_{S,opt} + B_{S,opt}$ ) that results in minimum noise factor. Your answer should be in terms of the intrinsic noise sources, and should be simplified. You may assume correlation coefficient c is imaginary and negative as we did in lecture.
- c) Find an expression for the noise factor when  $Y_S = 1/50\Omega$ . Your answer should be in terms of the intrinsic noise sources, and should be simplified.