Multimode 2.4 GHz Front-End With Tunable g_m-C Filter

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***Abstract*—We present a wireless front-end in a 1.2V 0.13µm CMOS technology. This receiver is designed for use with 2.4GHz RF frequencies such as Bluetooth, IEEE 802.11 (WiFi), or IEEE 802.15.4 (ZigBee). A low-noise amplifier (LNA), mixer, and tunable g_m-C filter are the components discussed in this document.**

***Index Terms*—Bluetooth, LNA, Tunable g_m-C Filter, Wifi, ZigBee, 802.11**

INTRODUCTION

UNALLOCATED frequencies of the RF spectrum, called the industrial, scientific, and medical (ISM) band, have proved to be useful for WPANs and short-range wireless communication applications. Among these communication methods are Bluetooth, WiFi, and ZigBee. The aforementioned methods operate at a 2.4GHz carrier frequency. The number of devices that are using wireless communication is increasing with the increasing popularity of wireless communication.

This report will describe the design methodology and functionality of three crucial components of any wireless communication receiver: a Low Noise Amplifier (LNA), Mixer, and channel select filter (a g_m-C filter in this work). In any wireless communication receiver, an antenna (not part of this work) receives a modulated RF signal, which is then fed into the LNA. The LNA is an amplifier with a low noise figure so that the overall noise figure as predicted by the Friis equation will be low. The output of the LNA is fed into a mixer, which performs the task of demodulation with the help of a local oscillator (not part of this work). Finally, a g_m-C filter (possibly with variable gain) is tuned for a specific channel of the transmitted band and the output is what was transmitted before modulation and transmission.

Ideally, a front-end will have a high linearity, a low noise figure, and provide gain. Figure 1 shows the system-level implementation of this work. All components have been optimized for operation at 2.4 GHz.

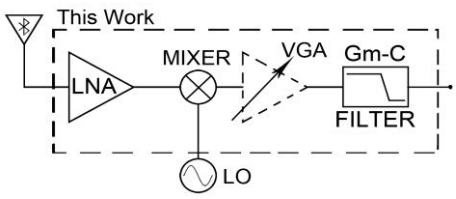

Fig. 1: System-Level Diagram

LOW-NOISE AMPLIFIER

The first stage of the receiver consists of a single-ended LNA and a single-ended to differential converter. A single-ended LNA was chosen to improve system noise performance. As the first element in the system, noise from the LNA is directly added to the noise of the overall system as predicted by the Friis equation. A single-ended to differential converter is needed for the input to the double balanced mixer.

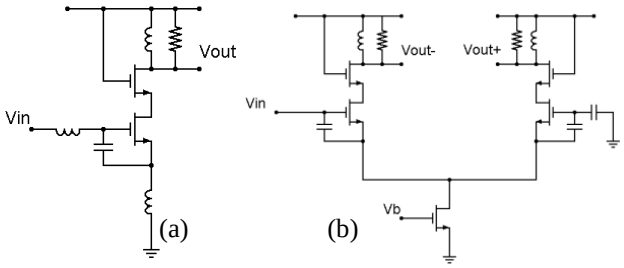

Fig. 2: (a)LNA and (b)Single-to-Differential Schematics

Design Methodology

An inductively degenerated cascode topology was chosen as a means to provide an input match of 50Ω. S11 was minimized for this 50Ω environment. The current density method of LNA design was used to find initial device sizing. The desired input impedance and device length is chosen and this determines the other parameters in the circuit. Input impedance of the amp as in [11] can be show to equal:

$$Zin = \frac{1}{sC_{gs}} + s(Ls + Lg) + \frac{g_m}{C_{gs}}Ls \qquad (1)$$

From this starting point, simulation was used to further tune component values. An additional capacitor, C_{ex}, across the gate and source of the input transistor was added to increase the size of the degeneration inductor to manufacturable sizes. In the above equation, C_{gs} is replaced by $C_{tot} = C_{gs} + C_{ex}$. Fig. 3 shows the measured results of the LNA and single-to-differential stages.

Single-to-differential Circuit

The mixer requires a differential RF signal input, thus necessitating a single-ended to differential converter. A fully differential amplifier was designed for this stage. Half circuit analysis was used in this design, though does not hold due to the single input. The second input of the amplifier is AC grounded.

To determine the input impedance of the single-ended to differential converter, a sine wave was input to the amplifier. From the transient voltage and current plots, the magnitude

and phase of the impedance can be found. Using the assumption that the input will be a parallel RC circuit, the magnitude and phase measurements lead to a purely capacitive input. This capacitance was too small to resonate out with a reasonable LNA load inductor. A capacitor placed across the gate and source of the input transistor decreases the size of the LNA load inductor.

Design Challenges

The most difficult specification of the LNA to meet was IIP3. Gain of the LNA was high in order to cancel noise in both the mixer and the filter. At high input levels, this high gain would cause the transistors to leave the saturation region and distort the signal. A load resistor was added to cut down gain. This increased the linearity, but decreased the bandwidth because of the gain-bandwidth product. Table 1 lists simulated LNA parameters and compares them with similar works.

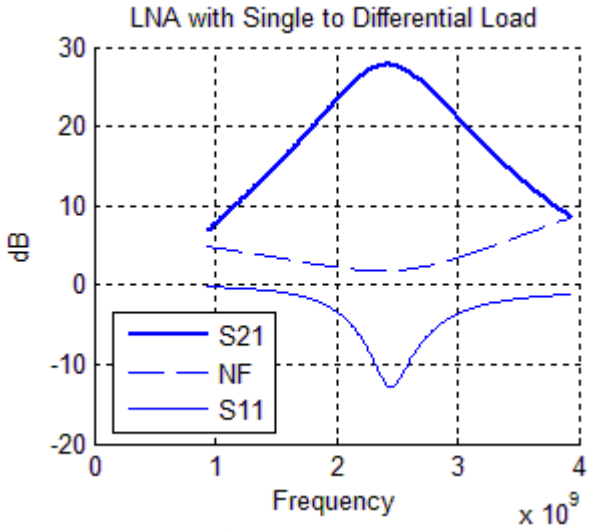

Fig. 3: Simulated LNA Performance

Table 1: LNA Performance

Specification	Targeted	Simulated	[8]	[15]
S21 (Gain)	>15 dB	28 dB	18 dB	15 dB
S11	--	-10 dB	-12 dB	-14 dB
NF	<5 dB	2.1 dB	4.8 dB	2.2 dB
IIP3	>-10 dBm	-20 dBm	--	.5 dBm
Power	<10 mW	2.77 mW	--	--

Matching the single-ended to differential converter and mixer was very difficult. When the mixer was attached, the single-ended to differential converter had much less gain and much more distortion than when simulated with a purely capacitive load. Sweeps of load capacitance did not generate the same measurements as with the actual mixer.

MIXER

Mixers perform the essential operation of down-mixing the RF signal to a lower frequency at which demodulation is much easier to perform. We chose to implement a variation of the Gilbert cell mixer, which is the most widely used topology.

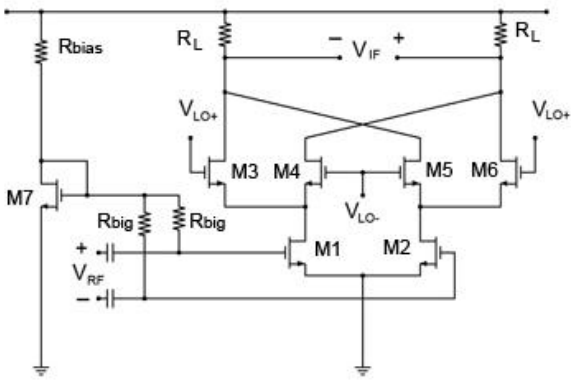

Fig. 4: Mixer Schematic

Design Choice

A Gilbert cell mixer was chosen because of its great port-to-port isolation and amplification. However, the typical tail current source may be omitted to improve linearity at the expense of common mode rejection. [15].

Transistors M_1 and M_2 act as transconductors, converting v_{RF} into a current which is then distributed between transistors M_3-M_6 in a commutating fashion. The local oscillator is set up to allow either [M_3 and M_6] or [M_4 and M_5] to be on at any given time. This action leads to a multiplication of RF and LO signals and is the basis of mixer operation.

Conversion Gain

The conversion gain of a mixer is the ratio of the IF signal to the RF signal. Assuming a Square LO signal from 0 to 1, we can realize this as a signal multiplication and use a Fourier transform of the LO signal for our analysis.

$$v_{IF} = A_{RF}\cos(\omega_{RF}t)\,\mathcal{F}(v_{LO}) \quad (2)$$

Where $\mathcal{F}(v_{LO})$ is the Fourier series expansion of the square wave LO signal given by

$$\mathcal{F}(v_{LO}) = \frac{1}{2}\left[1 + \frac{4}{\pi}\cos(\omega_{LO}t) + \frac{2}{3\pi}\cos(3\omega_{LO}t) + \cdots\right] \quad (3)$$

$$v_{IF} = \frac{1}{2}A_{RF}\cos(\omega_{RF}t) + \frac{2}{\pi}A_{RF}\cos(\omega_{RF}t)\cos(\omega_{LO}t) + \cdots \quad (4)$$

The mixing term gives a conversion gain of $G_C = \frac{2}{\pi}$, resulting in a total gain $A_{RF-IF} \approx \frac{2}{\pi}(g_{m,M1,2}R_L)$ from the differential common source configuration of M1 and M2. Active mixers are desirable because they provide gain, which reduces the noise figure contributed by following stages. Fig. 5 shows the conversion gain and noise figure as LO power varies.

Noise

Noise analysis of mixers can be a tedious task. Aside from the noise contribution at the IF output, noise is modulated down from odd harmonics of ω_{LO} and adds to the noise figure. Another major contributor to noise is the IF frequency at which the signal is demodulated. In direct-conversion receivers such as ours, flicker noise is dominant at the IF frequency. This also leads to an increased overall noise figure. Fig. 6 shows two distinct noise peaks at ω_{LO} and $3\omega_{LO}$ as well

as 1/f flicker noise. Noise Figure simulations were simulated at 500kHz since it lies within the bandwidth of a single Bluetooth channel.

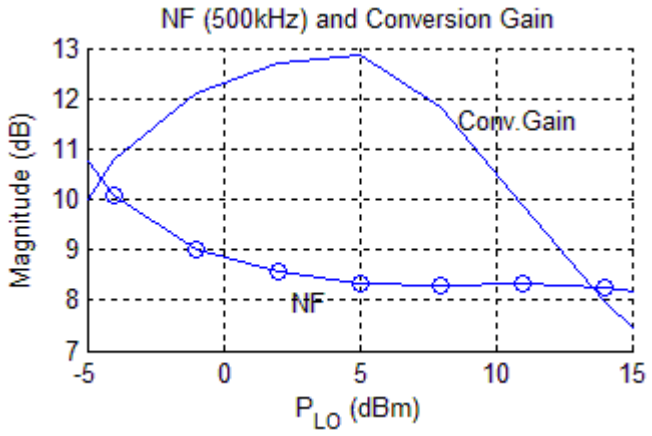

Fig. 5: Mixer Gain and NF

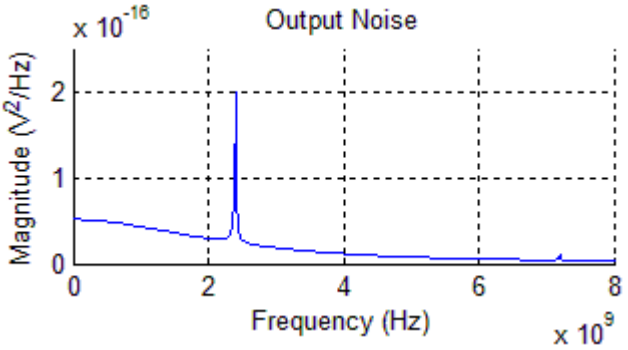

Fig. 6: Mixer Output Noise

Design Challenges

Because their operation is based on nonlinear principles, mixers may be difficult for the first-time designer to comprehend and simulate. Flicker noise is significant in direct-conversion receivers; reducing the noise figure of the mixer was the most challenging part of the design. Initially, with a tail current source, 750µA of total current was flowing through transistors M1 and M2. Once the tail current source was removed, there was more headroom and the length of the transistors was increased. Increasing R_L, DC bias current and g_m of M1 and M2 all improved noise factor.

Table 2: Mixer Performance

Specification	Targeted	Simulated	[18]
NF	< 14 dB	8.4 dB	22 dB
IIP3	> -10 dBm	-2.24 dBm	16.5 dBm
Power	< 10mW	8.34 mW	1.5 mW

G_M-C FILTER

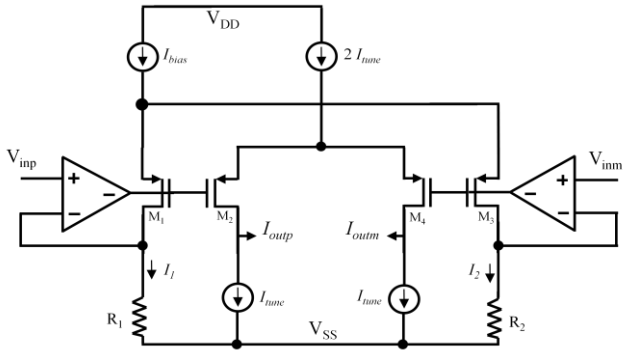

Fig. 7: Transconductor

The g_m-C filter was based entirely on [1], which is a third order Butterworth filter manufactured in a 180nm standard CMOS process by TSMC. We were attracted to this architecture due to its low-power consumption, wide tuning range, and use of translinear loops in subthreshold.

The primary devices of the transconductor (g_m) stages are devices M1-M4, and would have an exponential dependence on V_{gs}, and thus form a translinear multiplier loop which is linearly scalable by adjusting the bias through M_2 & M_4. If I_1 is the current through M_1 & R_1 (also M_3 & R_2), I_{tune} the current through M_2 (M_4), the small-signal output current i_o is given by:

$$i_o = \frac{I_{tune}}{I_1} i_i \qquad (5)$$

…where i_i is the change in M1 current due to V_{in}.

Long channel lengths and large aspect ratios are required for the necessary output resistance and current drive, however our process did not lend itself well to subthreshold design for two primary reasons: first, we are not in a digital CMOS but an RF process where, because carrier mobility is a high priority, substrate doping is kept low. This means as channel length increases and the average channel doping from halo implants approaches the bulk concentration, V_{th} exhibits a severe rolloff. Second, in order to achieve the desired tuning ratio of 50-100, one must have two decades of current variation achievable in the good subthreshold slope region. This coupled with a low V_{th} for long channel devices means that device sizes must be exponentially larger than a digital process with less V_{th} rolloff at long lengths. Ultimately it was decided to abandon subthreshold and design with devices in saturation.

Another difficult aspect of the transconductor was the feedback loop controlling the primary voltage to current conversion (opamp through M_1 & R_1). The parasitic gate-drain capacitance of M_1 forms a right-half-plane zero that causes a steep phase decline, reversing the polarity of feedback before unity gain. We successfully compensated these parasitics, but ultimately the transconductance was not linear enough in subthreshold due to the subthreshold slope issues mentioned above and feedback stabilization criteria.

In saturation, neglecting short channel effects, and assuming the threshold voltages of M_1 – M_4 are identical, the Taylor series expansion of the output current is as follows:

$$I_o = \frac{\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}}{R} - V_{in}\left[\frac{\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}}{R\sqrt{1-4AkR\left(\frac{W}{L}\right)_1(V_s+V_{th})}}\right] - Vin^3\left[\frac{A^4k^2R\left(\frac{W}{L}\right)_1\left(\frac{W}{L}\right)_2}{2\left(1-4AkR\left(\frac{W}{L}\right)_1(V_s+V_{th})\right)^{\frac{5}{2}}}\right]$$

…where A is the gain of the feedback opamp, *R* is R_1 or R_2, and *k* the MOS device parameters. As *Vs* also appears in the expansion, care was taken to bias the source voltages of each pair as closely as possible.

While we were not able to completely assemble[1] the gm-C filter due to our last minute change in the transconductor design, we achieved the following performance from the transconductor:

Table 3**: Transconductor Performance**

Specification	Targeted	Simulated[2]	[1][3]
Gain	>0 dB	3 dB	0 dB
IIP3	> -18 dBm	-1.62 dBm	22.3 dBm
Max g_m	100µS	206.2µS	100µS
Input-Referred Noise Density	< 1µV/√Hz	355.4 nV/√Hz	425 nV/√Hz
Power	< 1.5 mW	1.42 mW	< 1mW

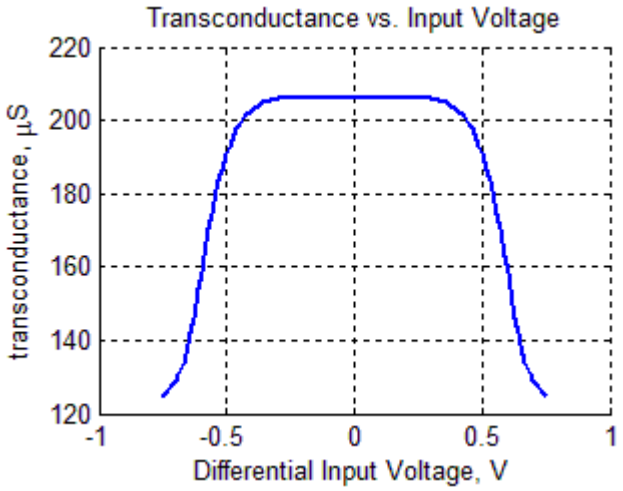

Fig. 8: Transconductance

LAYOUT

Fig. 9 shows the layout of our circuit. Note that only one gm-C cell is shown. The area for each block is as follows:

I. *LNA*
   a. LNA 0.99mm^2
   b. Single to differential converter 1.075 mm^2
II. *Mixer* 0.0152mm^2
III. *Transconductor*
   a. Core, with two opamps 6844.32 µm^2
   b. CMFB cell 2250 µm^2

[1] We assembled and biased the entire filter, but its gain was insufficient.

[2] Our transconductor was measured with 10pF on each differential output, which is more load than it would see in the filter.

[3] Gain, IIP3, and Noise Density for entire filter. Power for individual transconductor is no more than 1/7th of the reported total 4.1mW.

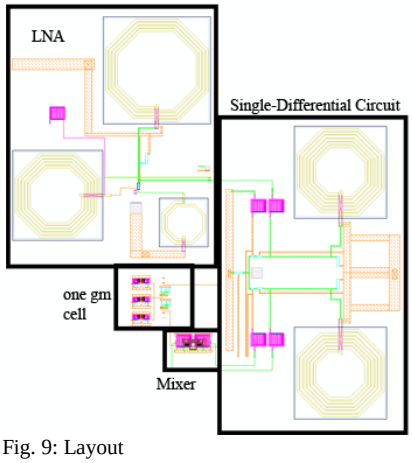

Fig. 9: Layout

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