

EECS 598 Fall 2013

VLSI Digital Signal Processing Systems

Instructor: Zhengya Zhang
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Lectures: MW 1:30 – 3:00 pm, 1008 EECS

Prerequisite: EECS 427 (VLSI Design I) or permission of instructor

Grading: 40% Topic surveys and presentations (or design project)
40% Term paper
20% Evaluation of peer work

Course Description:

Digital signal processing (DSP) systems have been enabled by the advances in very-large scale-integrated (VLSI) technologies. New DSP applications constantly impose new challenges on VLSI implementations. These implementations must satisfy real-time constraints imposed by the applications and must fit increasingly stringent area and power envelope. This course will survey methodologies needed to design efficient and high-performance custom or semi-custom VLSI systems for DSP applications. The primary focus of the course is on design of architectures, algorithms, and circuits, which can be operated with small area and low power consumption to deliver a high speed and functional performance.

Topics:

Introduction to Digital Signal Processing Systems
Iteration Bound
Pipelining and Parallel Processing
Retiming
Unfolding and Folding
Systolic Architecture Design
Algorithm Strength Reduction
Scaling and Roundoff Noise
Low-Power Design
Applications in Communication Systems and Signal Processing Systems