Nanometer Device Scaling in Subthreshold Circuits

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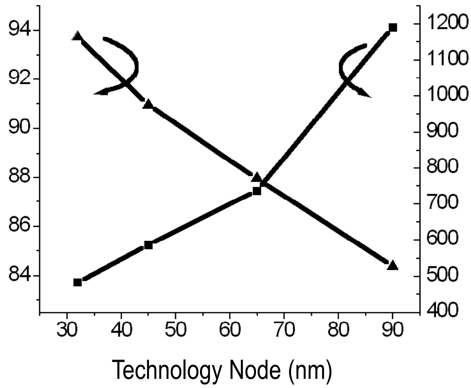

Slow gate oxide scaling leads to degradation of inverse subthreshold slope (S_S) and I_{on}/I_{off}.

Subthreshold circuit design is promising for future ultra-low-energy sensor applications, as well as highly parallel, high-performance processing. Device scaling has the potential to increase speed in addition to decreasing both energy and cost in subthreshold circuits. In this work, we use 2-D device simulations to investigate the implications of device scaling on subthreshold logic and SRAM and find that current scaling trends will create several key problems in low-voltage circuits. In particular, we find that the slow scaling of gate oxide thickness leads to a 60% reduction in I_{on}/I_{off} between the 90nm and 32nm device generations (as shown in the figure above). Our work further explores the effects of this device degradation on noise margins, delay, and energy. Using these observations of expected scaling trends, we propose an alternative scaling strategy that specifically targets subthreshold operation and demonstrates significant improvements in noise margins, delay, and energy in sub-V_{th} circuits. Using both optimized and unoptimized subthreshold device models, we explore the robustness of scaled subthreshold SRAM. We use a simple variability model and find that even small memories become unstable at advanced technology nodes. However, the simple device optimizations suggested in this work can be used to improve nominal read noise margins by 64% at the 32nm node. While it is unlikely that foundries will begin offering subthreshold-optimized devices in the near future, our work is important because it identifies sound design practices for subthreshold circuits designed in conventional scaled technologies. This project is supported by the Engineering Research Centers Program of the National Science Foundation under award number EEC-9986866.